

# Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off

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**Abstract**—This paper presents a new approach for power amplifier design using deep submicron CMOS technologies. A transformer based voltage combiner is proposed to combine power generated from several low-voltage CMOS amplifiers. Unlike other voltage combining transformers, the architecture presented in this paper provides greater flexibility to access and control the individual amplifiers in a voltage combined amplifier. In this work, this voltage combining transformer has been utilized to control output power and improve average efficiency at power back-off. This technique does not degrade instantaneous efficiency at peak power and maintains voltage gain with power back-off. A 1.2 V, 2.4 GHz fully integrated CMOS power amplifier prototype was implemented with thin-oxide transistors in a 0.13  $\mu\text{m}$  RF-CMOS process to demonstrate the concept. Neither off-chip components nor bondwires are used for output matching. The power amplifier transmits 24 dBm power with 25% drain efficiency at  $-1$  dB compression point. When driven into saturation, it transmits 27 dBm peak power with 32% drain efficiency. At power back-off, efficiency is greatly improved in the prototype which employs average efficiency enhancement circuitry.

**Index Terms**—CMOS, efficiency, integration, linearity, power amplifier.

## I. INTRODUCTION

TODAY'S consumers demand wireless systems that are low cost, power efficient, reliable and have a small form-factor. High levels of integration are desired to reduce cost and achieve compact form factor for high volume applications. Hence, the long term vision or goal for wireless transceivers is to merge as many components as possible, if not all, to a single die in an expensive technology. Therefore, there is a growing interest in utilizing CMOS technologies for RF power amplifiers (PAs) [1]. Although several advances have been made recently to enable full integration of PAs in CMOS, it is still among the most difficult challenges for achieving a truly single-chip radio system in CMOS. This is exacerbated by supply voltage reduction due to CMOS technology scaling and on-chip passive losses due to the conductive substrate used in deep-submicron CMOS processes.

Efficiency is one of the most important metrics for the design of power amplifiers. Conventional designs give maximum efficiency only at a single power level, usually near the maximum

rated power for the amplifier. As the output power is backed off from that single point, the efficiency drops rapidly. However, power back-off is inevitable in today's wireless communication systems. First, the need to conserve battery power and to mitigate interference to other users necessitates the transmission of power levels well below the peak output power. Transmitters only use peak output power when absolutely necessary. In many situations, PAs are operating at 10–20 dB back-off from peak power. Second, the requirement for both high data rate and efficient utilization of the increasingly crowded spectrum necessitates the use of both amplitude and phase modulation. Furthermore, in a number of wideband applications, robustness to multipath and SNR optimization over a wide bandwidth necessitate a large number of carriers with low data rates over a single carrier with a high data rate. For example, IEEE 802.11a/g uses orthogonal frequency division multiplexing (OFDM) which employs 52 sub-carriers at maximum data rate. The resultant composite signal has a large peak-to-average power ratio.

To date, there has been relatively little research on the design of a CMOS PA targeting good average efficiency. A new transformer combining architecture, which is suitable for designing highly efficient PAs in CMOS processes, is proposed to address the efficiency degradation at power back-off. It enables the control and access to individual amplifiers in a power combined amplifier. This feature is utilized in this work to improve efficiency at power back-off. A fully integrated CMOS prototype has been implemented to verify the concept [2]. Here a more in-depth treatment of the proposed transformer architecture and the design of the prototype are reported. This paper is organized as follows. Section II presents the on-chip transformer architecture proposed in this work. Section III describes the design of the prototype. Experimental results are presented in Section IV.

## II. POWER CONTROL AND AVERAGE EFFICIENCY ENHANCEMENT

Many combining approaches have been developed before, such as series stack combining [3], [4], and transmission line based combiner [5]. Among them, transformers have been widely adopted as a means for splitting and combining RF power [6], [7]. For example, a circular-geometry distributive active transformer, known as DAT, functions as an eight-way power combiner in a CMOS PA implemented with 0.35  $\mu\text{m}$  CMOS transistors [8]. Fig. 1 shows the conceptual diagram of the proposed transformer architecture. An ideal four-way ( $N = 4$ ) power combined class-B amplifier is used here to demonstrate the concept. It is known that both output power and DC power of an ideal Class-B amplifier is inversely

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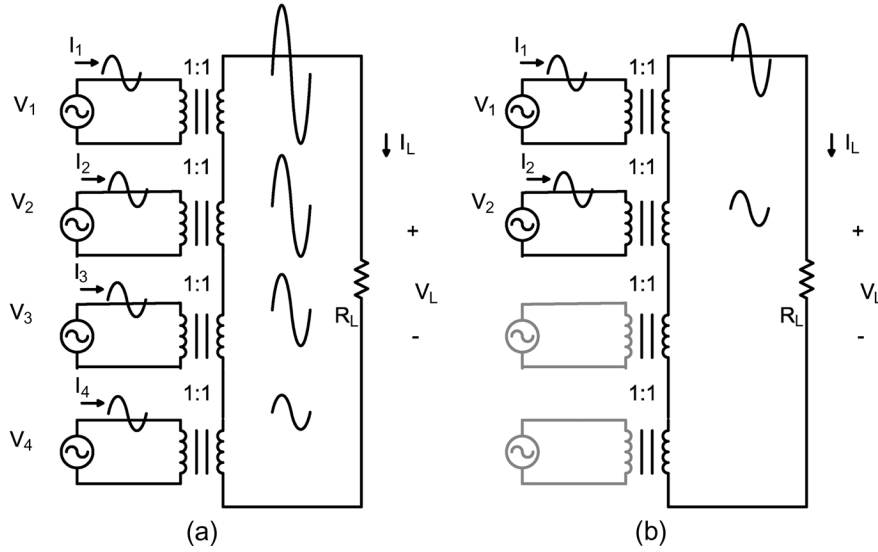


Fig. 1. Conceptual diagram of the transformer based power combining amplifier. (a) Peak power mode. (b) Power back-off mode.

proportional to the load  $R_L$ :

$$P_{\text{output}} = \frac{V_{\text{DD}}^2}{2R_L}$$

$$P_{\text{DC}} = \frac{2V_{\text{DD}}^2}{\pi R_L}$$

$$\eta = \frac{\pi}{4}.$$

The transformer will transform the load impedance to a lower value seen by each unit amplifier at the primaries and combine power generated from each unit amplifier at the secondary, using stacked 1:1 transformers. The primary sides of the four independent unity transformers are driven by four independent but synchronized sources with the same signal level in parallel. The secondary sides of the four independent unity transformers are stacked together in series. Assuming signal levels are equal on the primary sides, that is:

$$V_1 = V_2 = V_3 = V_4 = V_o.$$

Because the secondary sides are connected in series, the “ac ground” of the secondary side of each unity transformer is lifted so that the AC voltages add on the secondary:

$$V_L = V_1 + V_2 + V_3 + V_4 = 4V_o$$

The primary and secondary currents are equal and out of phase as the secondary side are connected in series:

$$I_1 = I_2 = I_3 = I_4 = I_L.$$

The impedance seen from the primary side of each unity transformer can be derived:

$$Z_1 = Z_2 = Z_3 = Z_4 = \frac{V_1}{I_1} = \frac{1}{4} \frac{V_L}{I_L} = \frac{1}{4} R_L.$$

The power delivered to the load is

$$P_L = \frac{1}{2} \frac{V_L^2}{R_L} = \frac{1}{2} \frac{(4V_o)^2}{R_L} = 8 \frac{V_o^2}{R_L}$$

and the power from each source is

$$P_1 = P_2 = P_3 = P_4 = \frac{1}{2} \frac{V_o^2}{Z_1} = \frac{1}{2} \frac{V_o^2}{\frac{1}{4} R_L} = 2 \frac{V_o^2}{R_L}.$$

Therefore, it is obvious that power is combined from each unity transformer and delivered to the load:

$$P_L = P_1 + P_2 + P_3 + P_4.$$

The focus of this work is the ability to control the output power of a transformer power combining amplifier and improve efficiency at power back-off. To do this, the primary side amplifiers must be controlled independently, which requires a new transformer layout and additional considerations. The proposed topology provides great flexibility during implementation, and enables access to and control of each unit amplifier.

As mentioned previously, an inherent problem with all traditional PA architectures is that one can only achieve maximum efficiency at a single power level, usually around the peak output power. As the output power is backed off from peak, the efficiency drops sharply. Various techniques have been proposed to improve efficiency at power back-off. The improvements are usually achieved by making PAs adaptive, such as varying bias current [9], supply voltage [10], or load impedance [5], [11]. Sometime, these techniques are combined to obtain better improvements in efficiency at power back-off. The Doherty technique [12] is probably the most well known technique that varies effective load impedance with power back-off, requiring a quarter-wave transmission line (or lumped equivalent) for functionality.

#### A. Dynamic Load Modulation

The proposed transformer topology has the unique property of being able to modulate the load seen by each unit amplifier. The principle of this dynamic load modulation is straightforward. The unit amplifiers are turned on or off as the required output power varies, controlled by a digital code (Fig. 2). At the

peak output power, each unit amplifier is on. Therefore, the load seen by each amplifier is

$$R = \frac{1}{4}R_L.$$

The efficiency of each amplifier, as well as the efficiency of the power combined amplifier, reaches maximum:

$$\eta_{\text{overall}} = \eta_{\text{unit}} = \eta_{\text{max}}.$$

The voltage gain of each amplifier is

$$A_{\text{unit\_voltage\_gain}} = g_m \cdot \frac{1}{4}R_L.$$

The total voltage gain of the power combining amplifier is

$$A_{\text{overall\_voltage\_gain}} = N \cdot A_{\text{unit\_voltage\_gain}} = g_m \cdot R_L.$$

The output voltage swing of each unit amplifier at peak output power is

$$V_o = V_{o,\text{max}} = A_{\text{unit\_voltage\_gain}} \cdot V_{i,\text{max}} = g_m \cdot \frac{1}{4}R_L \cdot V_{i,\text{max}}$$

and the peak output power is

$$P_{\text{out}} = P_{\text{peak}} = N \cdot P_{\text{unit\_peak}} = 4 \cdot \frac{1}{2} \frac{V_{o,\text{max}}^2}{\frac{1}{4}R_L} = 8 \frac{V_{o,\text{max}}^2}{R_L}.$$

When peak output power is not needed, the input drive is reduced to lower output power. When power is at 2.5 dB back-off, the input swing is reduced to  $3/4 \cdot V_{i,\text{max}}$ . At this point, the output swing of each individual amplifier is  $3/4 \cdot V_{o,\text{max}}$ . Therefore, the efficiency of each amplifier as well as the overall efficiency of the power combined amplifier drops. However, if one amplifier is turned off at this point, efficiency is enhanced. Since there are only three amplifiers ( $N = 3$ ) contributing to the output, a four-way power combined amplifier is reconfigured to a three-way power combined amplifier. The load seen by each active amplifier is now

$$R = \frac{1}{3}R_L.$$

The voltage gain of each amplifier increases to

$$A_{\text{unit\_voltage\_gain}} = g_m \cdot \frac{1}{3}R_L.$$

The output swing of each active amplifier returns to the maximum value

$$V_o = A_{\text{unit\_voltage\_gain}} \cdot V_i = g_m \cdot \frac{1}{3}R_L \cdot \frac{3}{4}V_{i,\text{max}} = V_{o,\text{max}}.$$

So the efficiency of the individual amplifiers and that of the power combined amplifier is given by

$$\eta_{\text{overall}} = \eta_{\text{unit}} = \eta_{\text{max}}.$$

The total voltage gain of the power combining amplifier is the same as before:

$$A_{\text{overall\_voltage\_gain}} = N \cdot A_{\text{unit\_voltage\_gain}} = g_m \cdot R_L$$

and the RF output power at this point is

$$P_{\text{out}} = N \cdot P_{\text{unit}} = 3 \cdot \frac{1}{2} \frac{V_o^2}{\frac{1}{3}R_L} = \frac{9}{2} \frac{V_o^2}{R_L} = \frac{9}{16} P_{\text{peak}}.$$

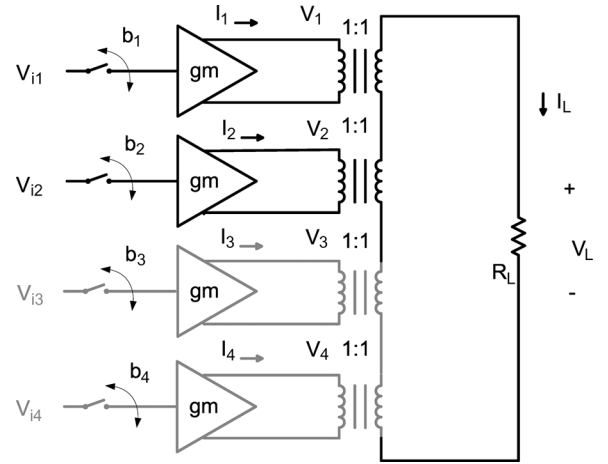


Fig. 2. Four-way power combining amplifier composed of four unit amplifiers.

One important feature is that the voltage gain remains constant as stages are turned on and off. Since the power is proportional to  $V^2$  and input matching and output load  $R_L$  are the same, the power gain remains constant as well. In practice, input matching might be affected as the stages are turned on and off. However, many measures could be taken to solve this issue. For instance, cascode devices are used in this work to turn on and off stages. Therefore, input matching remains the same as the power amplifier is reconfigured.

One additional unit amplifier could be turned off in order to improve efficiency at 6 dB back-off. In this case, a four-way ( $N = 4$ ) power combined amplifier is reconfigured to a two-way ( $N = 2$ ) power combined amplifier. At 12 dB back-off, only one amplifier need to be on ( $N = 1$ ). Therefore, the efficiency at power back-off is greatly enhanced, while the constant voltage gain is maintained as the power combining amplifier reconfigures. Fig. 3 shows the efficiency of a class-B power amplifier with an ideal power combining transformer.<sup>1</sup>

As the power combined amplifier reconfigures, the load of each unit amplifier varies. This is desirable from efficiency perspective, but it also raises concerns of reliability. Each transistor must be stable under the varying SWR presented by the effective load. From a current perspective, the devices are sized to drive the smallest load, and so under other conditions they have more than the needed capability when driving a larger load. Moreover, the advantage of the 1:1 voltage combining is the voltage on each transistor remains fixed which alleviates the concerns with voltage breakdown.

## B. Non-Idealities

To begin, transformer equivalent T-model, which has been covered extensively in the literature such as in [13], is briefly reviewed. The flux coupled transformers are often used for

<sup>1</sup>This topology is also suitable for other PA classes. For class-A biasing, the efficiency improvement is the same as the improvement obtained through adjusting bias current. However, voltage gain will change if the bias current is adapted. For class-AB biasing, especially for deeply biased class-AB, the efficiency improvement is similar as what can be achieved in class-B. For switching power amplifier, the efficiency improvement is the same as the improvement in class-B. Furthermore, this technique can be combined with other efficiency improvement techniques.

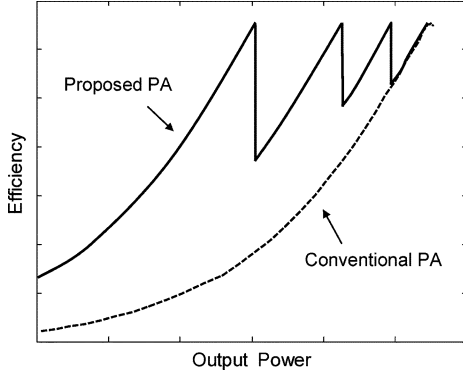


Fig. 3. Comparison of efficiency between the PA based on proposed power combining transformer and the conventional PA.

impedance matching, and on-chip transformers are usually implemented as coupled inductors. Therefore, non-idealities such as leakage flux, feed-through capacitance, and various losses cause real transformers to deviate from ideal behaviors. Fig. 4 shows the equivalent T-model of a transformer. Here  $L_1$  and  $L_2$  are the primary and the secondary inductor respective.  $R_1$  and  $R_2$  are resistors in series with the inductors to model their loss.  $K$  is the coupling factor and  $\alpha$  is the effective turn ratio, which is defined as

$$\alpha = \sqrt{\frac{L_2}{L_1}}.$$

In this model, the load,  $R_L$ , and a tuning capacitor  $C_2$ , are connected on the secondary side. The power efficiency of this transformer is of great interest in this work. The maximum efficiency of the transformer can only be achieved when it is tuned to resonance, and it is only determined by the quality factor of the coupled inductors  $Q_1$ ,  $Q_2$ , and the magnetic coupling factor  $k$ :

$$\eta_{\max} = \frac{1}{1 + \frac{2}{Q_1 Q_2 k^2} + 2\sqrt{\frac{1}{Q_1 Q_2 k^2} \left(1 + \frac{1}{Q_1 Q_2 k^2}\right)}}.$$

The maximum efficiency,  $\eta_{\max}$ , can only be obtained when the inductance of the primary coil is

$$\omega L_1 = \frac{A}{1 + A^2} \cdot \frac{R_L}{\alpha^2} \left( A = \frac{1}{\sqrt{\frac{1}{Q_2^2} + \frac{Q_1}{Q_2} k^2}} \right).$$

Ideally the efficiency should return back to its optimum value at the transition points; however, it inevitably degrades due to non-idealities of the power combining transformer. In the following discussion, several factors that cause the degradation will be examined with some proposed solutions.

First, the impact of the varying load on the efficiency of the power combining transformer is considered. Usually the inductance is chosen for the load condition at peak output power. As shown previously, the power amplifier is reconfigured at power back-off. Therefore, the load seen at the output of the unit amplifiers remaining “on” will vary. This will make the transformer

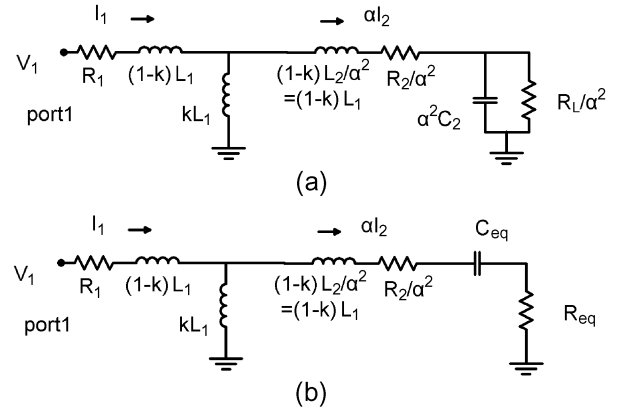


Fig. 4. (a) Transformer equivalent T-model with a load resistor and tuning capacitor. (b) Transformer T-model after parallel to series conversion at the load.

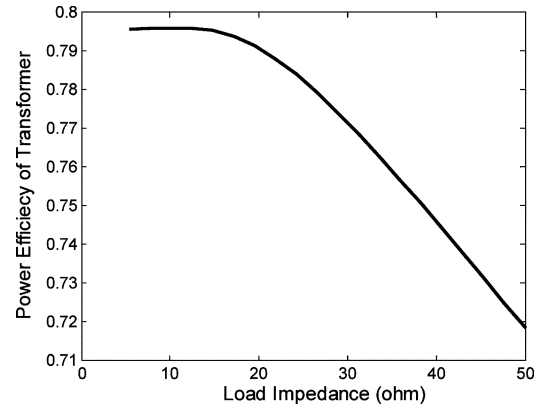


Fig. 5. Efficiency of an ideal power combining transformer as the load impedance varies. The transformer was designed to work with 12.5  $\Omega$  load (assuming  $Q = 12.5$ ,  $k = 0.7$ , at 2.4 GHz).

less efficient than in the peak power mode. Fortunately, the impact of varying load on the efficiency of the transformer is very minimal as shown in Fig. 5.

Next, the impact of loading of inactive unit amplifiers on the efficiency of the power combining transformer is considered. The power combining transformer is a passive device, which means it is bilateral. When the unit amplifiers are turned off, they will load the amplifiers that remain “on”. In this case, the power transfer efficiency from the secondary to the primary of the “off” stage should be minimized.

If the amplifiers that are turned off present an ideal open or short load to the voltage combining transformer, there will be no power transferred from the secondary to the primary of the off stages. This is highly desired in order to keep the efficiency high at back-off. However, in reality, the junction parasitics of the deactivated transistors are lossy, which will inevitably load the voltage combining transformer in an open state. This degradation can be minimized by switching out capacitors at the primary of the off stages to detune the unit transformers, and by shorting the terminals of the primary inductor. The loading presented to the secondary winding becomes an inductor in series with a small resistor. Simulations are used to verify the impact

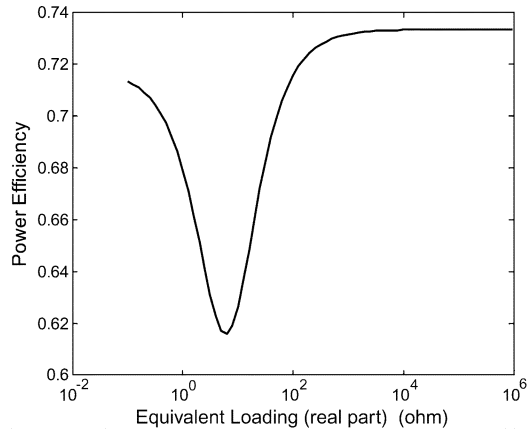


Fig. 6. Power efficiency of the implemented power combining transformer versus the loading from the deactivated unit amplifiers when the combiner is reconfigured from a four-way combiner to a two-way combiner. The equivalent loading is to model the effect of on-resistance of “shorting” transistors (results simulated with the s-parameter extracted from full-wave EM simulations).

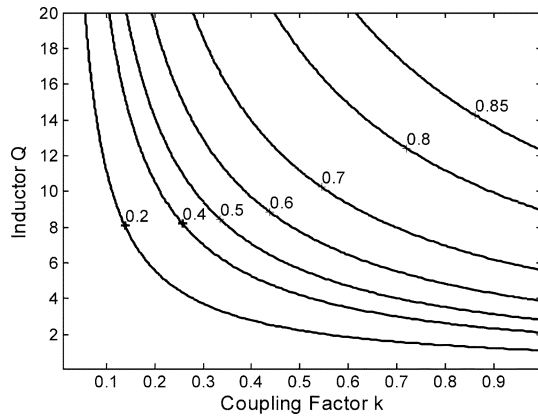


Fig. 7. Contour plot of constant power efficiency for a  $1:n$  transformer, assuming  $Q_1 = Q_2$ .

of the loading from off stages to the overall transformer power efficiency. The results are shown in Fig. 6.

The decision to “short” or “open” circuit the primary side of the off stages should be decided based on the actual implementation, such as process features, transistor sizes, and transformer design. In this work, it was found through simulations that “short” offers better efficiency at power back-off.

### C. Design of a Fully Integrated Power Combining Transformer in CMOS

The design of the fully integrated transformer is very dependent on the available process. Nonetheless, good power efficiency of the power combining transformer can be obtained by increasing the magnetic coupling factor and improving the quality factor of the coupled inductors (Fig. 7). While increasing magnetic coupling, capacitive coupling should be minimized as much as possible. In an RF-CMOS process, thick analog metal layers are usually available for designing high- $Q$  passives. For example, in an RF-CMOS process with dual analog metal layers, a simple overlay structure can be chosen to implement the power combining transformer.

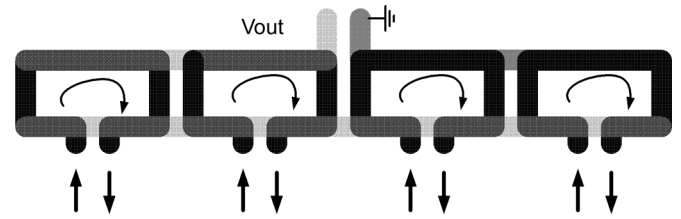


Fig. 8. Simple power combining transformer. Nonoverlapping segments of the primary and secondary reduces the coupling factor. The flow of current in opposite directions in these segments reduces the inductance and degrades the  $Q$  factors.

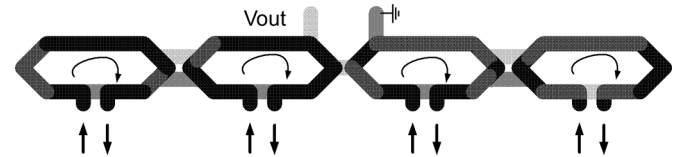


Fig. 9. Power combining transformer with reduced magnetic coupling between adjacent windings.

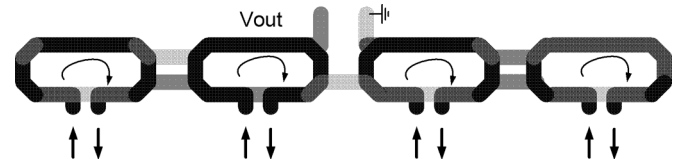


Fig. 10. Power combining transformer with oval-like high- $Q$  inductors.

A simple transformer layout is shown in Fig. 8. In this design, the adjacent windings have current flowing in opposite direction, and thus do not contribute as much flux and coupling to the secondary winding, reducing the power efficiency. Moreover, since the primaries will have different magnetic coupling to the secondary, a different load is seen at each primary which could severely degrade the performance.

Several measures can be taken to minimize coupling of the adjacent windings. One of them is to leverage the fact that orthogonal lines have negligible magnetic coupling as shown in Fig. 9. This layout still has one flaw, which is the degraded quality factor in the inductors arising from  $90^\circ$  corners. A compromise can be made as shown in Fig. 10, where the primary inductors are oval in shape and are physically separated further apart to minimize internal flux cancellation. This transformer was implemented with the prototype presented in Section III.

In a typical digital CMOS process, only one thick top metal layer is provided. Usually, this metal layer is thinner than the analog metal layer in an RF CMOS process. Therefore, a lateral coupling structure has to be employed which potentially degrades power efficiency from two aspects. First, the magnetic coupling is reduced compared to the overlay structure. Second, the inner inductor will suffer from current crowding which results from the proximity effect, just like in a multi-turn inductor. Consequently, the resistance of the structure increases and  $Q$  decreases.

A new “figure-8” style layout which can be implemented with a single thick top metal layer (Fig. 11) has been proposed to address these issues [14]. An interleaved structure is used for

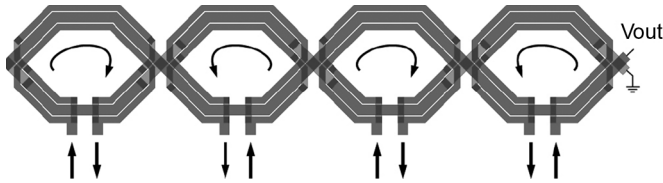


Fig. 11. Power amplifier with "figure-8" transformer power combiner.

TABLE I  
COMPARISONS AMONG STATE-OF-THE-ART  
POWER COMBINING TRANSFORMERS

Process	Type	Freq (GHz)	Efficiency	Area (mm <sup>2</sup> )	Ref.
GaAs	micro-strip line	2	0.877	1.2*1.2	[15]
0.35- $\mu\text{m}$ BiCMOS	micro-strip line	2.4	0.7	0.8*0.8	[8]
0.20- $\mu\text{m}$ SiGe	micro-strip line	21-26	0.776	0.4*0.2	[7]
0.18- $\mu\text{m}$ RF CMOS	micro-strip line	2.4	0.83	0.8*0.5	[16]
0.13- $\mu\text{m}$ RF CMOS	single-turn	2.4	0.8	1.8*0.25	[2]
90-nm CMOS	single-turn	5.35	0.75	0.65*0.15	[14]

the primary windings, to reduce losses and enhance magnetic coupling. An important additional benefit comes from the alternating direction of the secondary winding. The secondary winding is immune to common mode disturbance from a distant source, because the incoming magnetic flux induces currents of opposite directions across each "figure-8" section, assuming there is an even number of sections. The EM simulation of this structure shows an efficiency of 0.752 ( $IL = 1.35$  dB) at 5 GHz, with only one thick top metal in a 90 nm digital CMOS process.

In Table I, the performance of several power combining transformers are compared. Transformers composed of single-turn inductors demonstrate high power efficiency, comparable to transformers composed of microstrip line inductors. The ease of implementation, the compatibility with CMOS processes, and the ability of accessing individual amplifiers to improve average efficiency make transformers composed of single-turn inductors very appealing.

### III. FULLY INTEGRATED CMOS POWER AMPLIFIER PROTOTYPE

To verify the concepts outlined in this paper, a prototype power amplifier was designed and tested. There are generally many challenges associated with power amplifier design. Naturally, the output stage is the most challenging part of the design. Thus, the prototype is a single-stage CMOS PA utilizing standard thin-gate-oxide transistors in a 0.13  $\mu\text{m}$  CMOS technology. This process offers two thick upper metal layers, 3  $\mu\text{m}$  and 4  $\mu\text{m}$  thick respectively, over a conductive substrate (about 1  $\Omega\text{-cm}$ ). The  $f_T$  of the process is around 60 GHz. The top two

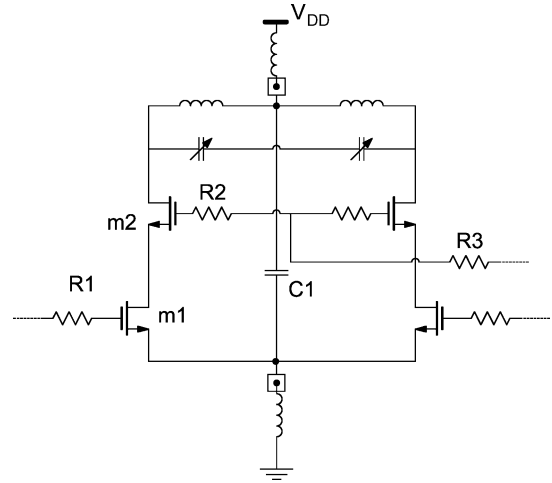


Fig. 12. Simplified schematic of a pseudo-differential pair.

metal layers are used to implement the integrated transformer. High-density MIM capacitors are also available in this process.

#### A. Pseudo-Differential Pair

A pseudo-differential pair serves as the main building block for the power amplifier. A single-ended topology is avoided to allow more robust integration. This topology creates an ac virtual ground at the common source node and  $V_{DD}$  supply node for the fundamental frequency and odd-order harmonics, minimizing the impact of package parasitics on amplifier performance. Each side of the pair drives a load down-transformed by a factor of two without incurring any additional loss. This is very important, since the on-chip matching network is usually lossy.

#### B. Cascode

To avoid degradation of RF performance, only standard thin-gate-oxide devices are used. The cascode configuration is used to improve reliability. The transconductor device (M1) and the cascode device (M2) have the same size (2400  $\mu\text{m}/0.16$   $\mu\text{m}$ ), so that they can easily share a junction to minimize the parasitic capacitance at the cascode node, improving the efficiency of the amplifier. The cascode gate is connected to the supply node when the individual amplifier is on, and it is grounded to turn off the individual amplifier for power back-off. Fig. 12 shows the simplified schematic of a pseudo-differential pair designed in this work. The simplified schematic of the prototype is shown in Fig. 13, in which four pseudo-differential amplifiers are combined.

#### C. Biasing

Class-AB biasing is chosen because both power efficiency and linearity are of primary concern in advanced wireless communication systems. In this work, the  $g_m$  of input devices is the major source of nonlinearity. It is known that when MOS devices are biased from the weak inversion region to the moderate inversion region,  $g_{m,3}$  changes polarity (from positive to negative). The input transistors are biased slightly above threshold to leverage this behavior. To reduce the inter-modulation products from mixing with the inputs and even-order harmonics, a large

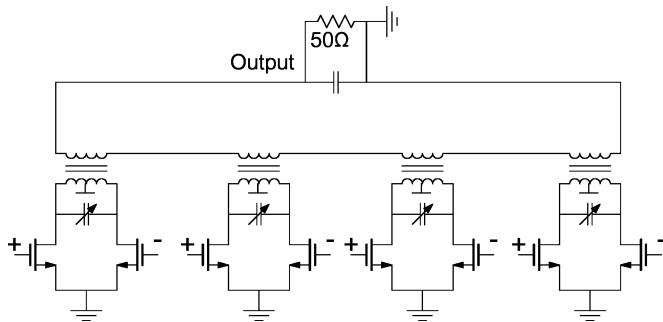


Fig. 13. Simplified schematic of the prototype.

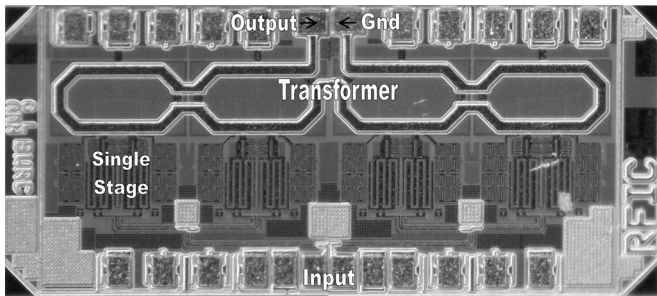


Fig. 14. Die microphotograph of the prototype.

on-chip bypass capacitor connects the center-tap of the transformer with the common source node. This significantly reduces even-order harmonics, and minimizes second-order interaction products from significantly contributing to the odd-order distortion [17]. For each unit amplifier, 60 pF bypass capacitor is used to reduce ripple on the supply nodes, implemented with MIM capacitors and finger capacitors.

#### D. Transformer and Matching Network

The transformer used in this work plays two roles. First, it is used to transform the  $50\ \Omega$  load. Second, it converts a differential signal into a single-ended signal so that it can be connected to the antenna directly. High efficiency of the transformer is the prerequisite in order to achieve high efficiency of the entire PA. High component  $Q$  and tight magnetic coupling are crucial to reduce the loss in the transformer. One-turn “hairpin” style inductors are implemented to construct the primary and the secondary coils of the transformer. To improve the magnetic coupling, an overlay structure is adopted wherein the secondary coil is put directly on top of the primary coils.

The power amplifier implemented in this work requires an eight-way power combining amplifier, to transmit 24 dBm linear power with 1.2 V supply voltage. Since pseudo-differential topology is adopted to implement the amplifiers, four pseudo-differential amplifiers and four 1:1 transformers are needed to construct an eight-way power combining amplifier (Fig. 10). Assuming that the achievable quality factors of both primary and secondary inductors are 12.5 and coupling factor is 0.7, the optimal inductance is around 400 pH at 2.4 GHz. A metal shield (M1) is used to reduce capacitive coupling to the conductive substrate. Fixed MIM capacitors are put on the secondary side to resonate out the secondary inductance to maximize efficiency. Switched MIM capacitors are put on the

primary side. When the stage is on, those capacitors are used to present an optimum tuned load to the transistors. When the stage is turned off, the capacitors are switched out to detune the unit transformer to improve overall efficiency. The “shorting” devices are implemented with nMOS transistors,<sup>2</sup> and are sized to give about  $0.5\ \Omega$  of on-resistance. The efficiency of the on-chip transformer is approximately 80%, simulated independently with Agilent ADS Momentum and Ansoft HFSS. The simulation results are in close agreement.

## IV. EXPERIMENTAL RESULTS

A microphotograph of the prototype is shown in Fig. 14. Fabricated using a  $0.13\ \mu\text{m}$  CMOS process, it features an eight-way ( $N = 8$ ) independent power combining amplifier, in which the inputs of the unit amplifiers are connected together and driven in parallel. The chip area is  $2\ \text{mm} \times 1\ \text{mm}$ , including pads. During measurements, the chip was directly glued to the printed circuit board using conductive adhesive. All the pads, including input and output pads, were wire bonded on the board. Each pad was bond-wired to the test board with only one bondwire, although multiple bondwires can be employed to minimize lead inductance. No off-chip impedance matching elements are needed or used in this design. The input is driven by a commercial driver amplifier through an off-chip balun. Since the input is not matched, power gain is not known exactly. It was estimated around 10 dB. The amplifier was tested with a 1.2 V power supply. The cascode node was tied to the power supply. The amplifier draws 114 mA DC current without RF signals applied.

#### A. CW Signal Test

The output was directly connected to a power meter with two 6 dB attenuators for power measurements. All system losses were calibrated out, while the measured results included losses of the PC board and bondwires. Output power and drain efficiency versus input power (read from the signal generator) for a single-tone test is shown in Fig. 15. The PA transmits up to 24 dBm linear power with 25% drain efficiency, centered at 2.4 GHz. When driven into saturation, it delivers 27 dBm power with 32% drain efficiency. Under the same bias conditions, a two-tone test was performed at 2.4 GHz with 1 kHz tone spacing. Little sideband asymmetry was observed during testing. The results are shown in Fig. 16. When the average output power per tone is 18 dBm, measured IM3, IM5, and IM7 are  $-29\ \text{dBc}$ ,  $-36\ \text{dBc}$ , and  $-42\ \text{dBc}$ , respectively.

To verify the concept of the average efficiency enhancement technique, two PAs are compared. They use the same devices and the same power combining transformer, with the exception that one employs the efficiency enhancement circuitry. Fig. 17 shows the measured results, in close agreement with simulation results.<sup>3</sup> With 1.2 V power supply, a peak power of 27 dBm is measured with 32% drain efficiency, when all of four amplifiers are “on”. When output power is at 2.5 dB back-off from peak power, in the PA employing average efficiency enhancement circuitry, one amplifier is turned off and the other

<sup>2</sup>PMOS transistors are preferred since source and drain are tied to  $V_{DD}$ .

<sup>3</sup>In the high output power region, the measured result differs from the simulated result because of the rise of chip temperature. All simulations are done with  $25\ ^\circ\text{C}$  temperature setting.

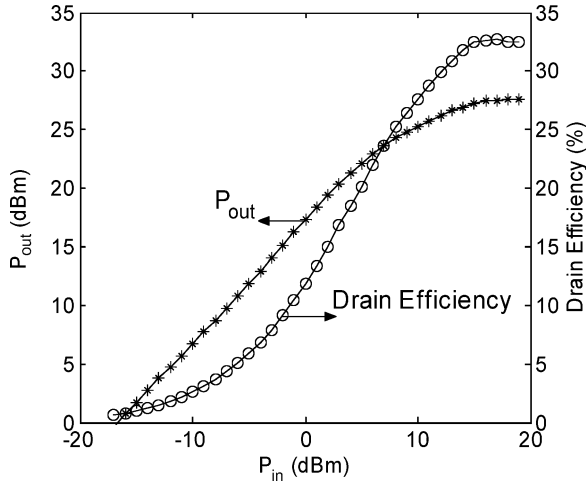


Fig. 15. Measured output power and drain efficiency from single-tone test.

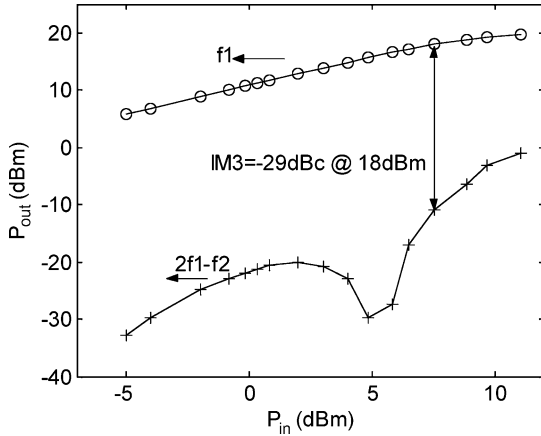


Fig. 16. Measured output power and IM3 from a two-tone test with 1 kHz tone spacing. The two input tones are combined using a combiner. The null of IM3 is from class-AB biasing [18].

three remain “on”. The drain efficiency is measured as 31.5% at 24.5 dBm, very close to the drain efficiency at peak output power. In contrast, drain efficiency is 5% lower in the conventional PA at 2.5 dB back-off. In fact, as shown in Fig. 18, further enhancements of efficiency in the back-off region can be obtained by turning off the remaining amplifiers sequentially, when output power is at 6 dB and 12 dB back-off. In this work, further improvements cannot be verified with experiments due to a design/layout mistake.

### B. Modulated Signal Test

Although the prototype was not designed to meet any particular standard, it was tested with EDGE and 802.11g signals to observe its linearity with modulated signals. Because automatic power control circuit was not implemented with the prototype, the improvement on average efficiency cannot be tested with modulated signals. However, the proposed technique, in principle, can potentially be used to enhance efficiency of a power

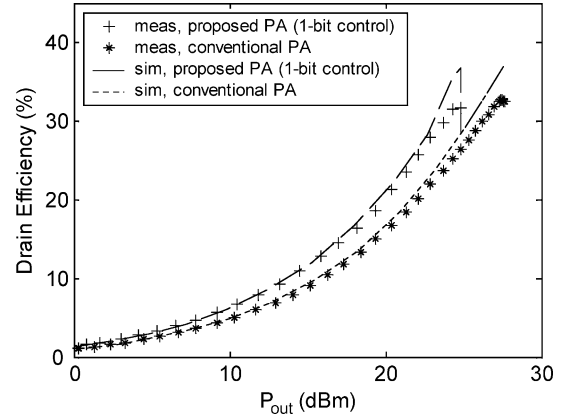


Fig. 17. Simulated and measured drain efficiency of the proposed PA, in comparison with those for the conventional PA.

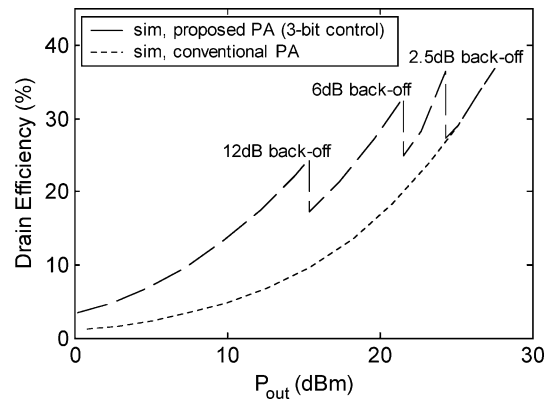
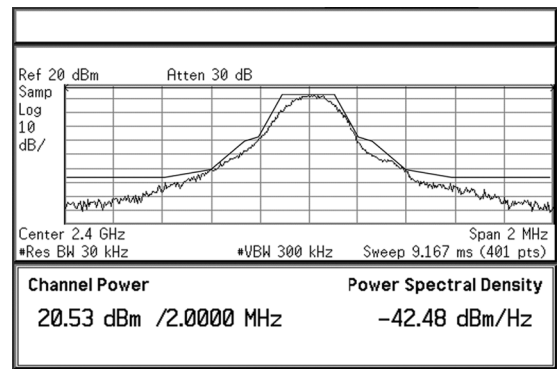


Fig. 18. Simulated drain efficiency of the proposed PA with power back-off, in comparison with that for the conventional PA.


 Fig. 19. Output spectrum with GSM/EDGE signal. Measured PSD at offset frequencies: at  $\pm 200$  kHz,  $-30.75$  dBc,  $-30.3$  dBc (spec:  $-30$  dBc); at  $\pm 400$  kHz,  $-55.3$  dBc,  $-55$  dBc (spec:  $-54$  dBc); at  $\pm 600$  kHz,  $-64.4$  dBc,  $-63.9$  dBc (spec:  $-60$  dBc).

amplifier when transmitting signals with high peak-to-average ratio (PAR).<sup>4</sup>

First, the PA was tested with GSM/EDGE signal, which provides high data rate over 200 kHz carrier bandwidth. In addition to Gaussian minimum shift keying (GMSK), EDGE uses

<sup>4</sup>In principle, the proposed structure can be used as a DAC. Issues such as quantization noise and clock feed-through need to be addressed to make the proposed structure work for high PAR signals.

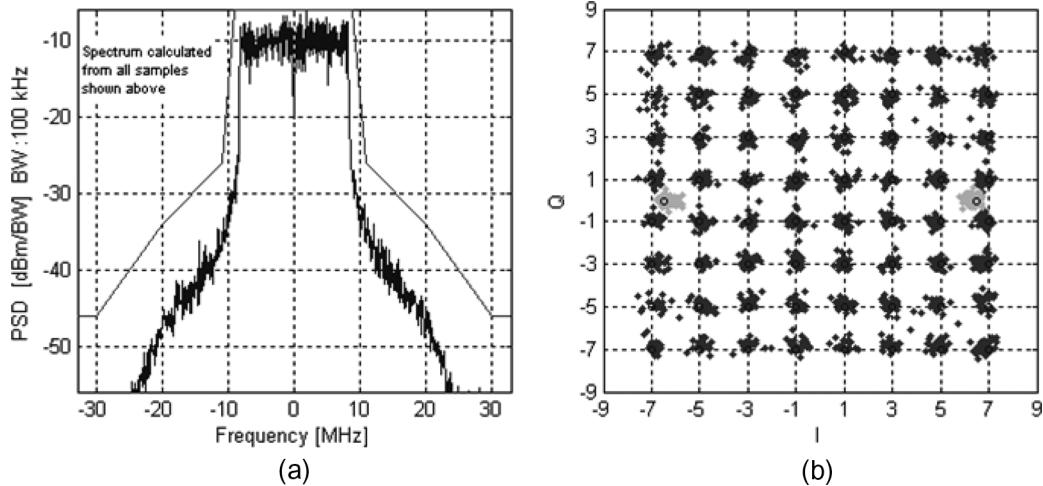


Fig. 20. Measured at  $P_{\text{out}} = 14.5$  dBm with 4.48% EVM. (a) Output spectrum. (b) Rectangular constellation diagram.

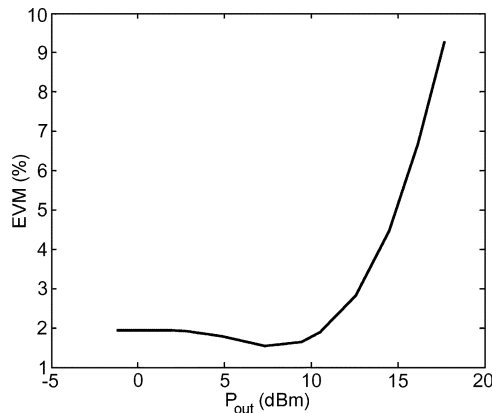


Fig. 21. Measured EVM versus output power.

8-phase-shift keying (8PSK) for the upper five of its nine modulation and coding schemes to achieve higher data rate than GSM. It has PAR of 3.2 dB, and peak-to-minimum ratio of 17 dB. The measured peak output power while still meeting the spectral mask is 21.75 dBm after calibrating out 1.25 dB cable loss (Fig. 19). The drain efficiency is 20%.

The prototype was also tested with 2.4 GHz 802.11g WLAN signal. Since the 802.11g OFDM symbol consists of 52 carriers (four pilot carriers), its amplitude PAR can be as high as 17 dB ( $10 * \log(52) \sim 17$  dB). However, such extreme peaks are in practice rare and brief. It is not necessary to preserve these extreme peaks in order to demodulate the signal correctly. The test signal from the signal source has 12 dB PAR at the data rate of 54 Mb/s using 64QAM modulation. The signal source was intentionally distorted with 1% EVM. The prototype delivers maximum output power 14.5 dBm with 4.48% EVM (Fig. 20). The drain efficiency is around 9%. Fig. 21 illustrates measured EVM with the PA output power. Simple AM-to-PM predistortion can improve the performance considerably, and allow operation closer to the compression point.

## V. CONCLUSION

In this paper, a simple yet elegant technique was described to achieve high efficiency at peak power as well high average efficiency. Topologies suitable for implementation in CMOS tech-

nologies are studied. A prototype fabricated with only thin-gate-oxide transistors in a 0.13  $\mu\text{m}$  CMOS technology demonstrates the concept. With 1.2 V supply, it transmits linear power up to 24 dBm with 25% drain efficiency. When driven into saturation, it transmits 27 dBm peak power with 32% drain efficiency. As one of the four amplifiers is turned off for 2.5 dB power back-off from 27 dBm, drain efficiency is improved from 26.5% to 31.5%, very close to instantaneous drain efficiency at peak power.

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