A 6-b DAC and Analog DRAM for a Maskless Lithography Interface in 90 nm CMOS

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***Abstract*- A parallel, 12μm-pitch, low-power 6-b segmented digital-to-analog converter (DAC) array drives an array of 3μm × 3μm analog DRAM cells in a 2.5/1V 90 nm CMOS process, with an application in maskless lithography. An innovative self-calibrating compensation circuit limits the effect of charge leakage and capacitive process mismatch to less than 0.5LSB over 100ms of data hold time. A 2mm x 2mm test chip implements a mixed-signal interface with 32 DACs driving four 32 × 256 analog DRAM arrays.**

I INTRODUCTION

As minimum feature sizes in CMOS technology scale, the cost of critical dimension masks dramatically increases. Although the masks are still a small fraction of the overall cost of the large-volume chip development, they present a significant impediment to low-volume ASICs, and increase the cost of prototyping and process development. To alleviate the cost of low volume fabrication, alternatives to mask-based optical lithography have been pursued. Various approaches to maskless lithography have been investigated in the past: e-beam, micro-machined mirror projection, and nano-jet printing. Recent updates of the International Technology Roadmap for Semiconductors (ITRS) predict existence of maskless lithography as an alternative to conventional mask-cased optical lithography in sub-45nm technology nodes [1].

A promising technology for maskless lithography systems is based on spatial light modulators (SLM). In this approach, micro-mirror based system modulates the position of individual mirrors in the array to create the image based on its corresponding diffraction pattern. The advantage of this system is in its compatibility with optical lithography tools, where a fixed mask would be replaced with a programmable one [2]. A feasibility of this approach has been demonstrated on existing mask-writing tools that use the same technology [3]. The mask writer system is based on a 512 × 2048 array of 16μm × 16μm MEMS mirrors. The mirrors are tilted in 256 different steps through analog voltages provided by an external array of 128 DACs. Although acceptable for mask writing, the speed of this system is several orders of magnitude below the requirements for maskless lithography.

To upgrade the SLM-based mask writing process for use in maskless lithography, the throughput needs to be dramatically increased, [4]. To achieve a 1nm edge placement using 22nm pixels targeted for a 45nm process technology, 5-bit grayscale data per pixel representation is needed, [5]. This results in a total of 500Tb of information on a 300mm wafer. Prototyping and low-volume ASIC production can be made economically viable with 1-6 wafer layers per hour [2], requiring data throughputs of up to 1.6Tb/s. Besides overcoming the challenges of handling large volumes of data, the maskless lithography system has to be able to integrate a large array of small-dimension nanomirrors. A key challenge of building this custom silicon chip is the need to bring a large number of DACs on chip and to store the analog control voltages underneath the mirrors. In this paper, we present a mixed-signal interface to the mirror array, designed in 2.5V/1V 90nm CMOS technology satisfying the requirements for exposing up to 3 wafers/hour.

II SYSTEM ARCHITECTURE

Figure 1 illustrates a maskless lithography system based on an SLM with a nanomirror array to generate the mask patterns. In this approach, the reconfigurable mask forms a new pattern between consecutive light flashes. The mirror-controlling voltages must be loaded between the flashes and stored in an analog memory array. The memory array connects to the electrostatically controlled mirrors to adjust their individual positions. The 3μm×3μm polysilicon mirrors positioned to a minimum of 32 levels can achieve 22nm feature sizes with a 1nm edge placement through a 140× optical reduction [6]. The mirrors can be either piston or tilting type [7-8], and the size of array requires the integration of driving electronics onto the SLM chip. Our design demonstrates the feasibility of an analog interface to the nanomirror array, capable of storing and maintaining precise voltage based position data between the laser flashes.

To achieve the desired throughput of 3wafers/hour requires 12 million pixels to be exposed in each flash. The mirrors would be placed in a 6,144×2,048 array, driven by parallel DACs from each side, Fig. 2. To accommodate for various errors, the DAC resolution would be 6 bits, and has to be able to load at least one row of 1,024 mirrors in 100μs between the flashes.

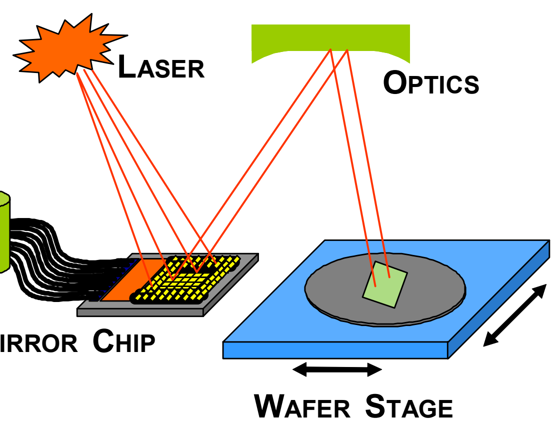

Fig. 1. SLM-based maskless lithography system.