Modeling Advanced FET Technology in a Compact Model

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Invited Paper

***Abstract*—The need for meeting the expectations of continuing the enhancement of CMOS performance and density has inspired the introduction of new materials into the classical single-gate bulk MOSFET and the development of nonclassical multigate transistors at an accelerated rate. There is a strong need to understand and model the associated new physics and electrical behavior to ensure widespread very-large-scale-integration circuit applications of new technologies. This paper presents some of the efforts toward the modeling of new technologies for bulk MOSFETs and multigate transistors. A holistic model for mobility enhancement through process-induced stress and a dynamic behavior model for high-k transistors have been developed to capture some of the new effects and new materials in the bulk MOSFET. A new analytical model is also presented for the fundamentally new device structure—FinFET.**

***Index Terms*—Berkeley short-channel insulated-gate FET model (BSIM), compact modeling, dielectrics, double-gate MOSFETs (DG-MOSFETs), high-k, MOSFET, process-induced strain.**

I. Introduction

Bulk CMOS scaling has been the traditional workhorse of the semiconductor industry to achieve constant enhancement in current drive, which leads to faster and smaller chips [1]. In the last few years, as the bulk MOSFET scaling is starting to slow down, the industry has started chartering two different paths [2], [3]. The first path involves the introduction of new technologies and new materials into the classical single-gate bulk MOSFET. New materials are being introduced into the bulk transistor to create uniaxial and biaxial stress in the inversion channel, leading to higher electron and hole mobilities and, hence, higher current drives [4], [5]. High-k dielectrics are being introduced to meet the required effective gate capacitance with a larger physical insulator thickness to control the gate leakage tunneling current [6]. The second path in achieving higher CMOS performance is to use nonclassical structures with more than one gate electrode [7]–[9]. Multigate transistors have a strong potential to extend the CMOS scaling into the sub-25-nm regime. In this paper, the modeling of the changes in electrical behavior due to the aforementioned technologies is presented.

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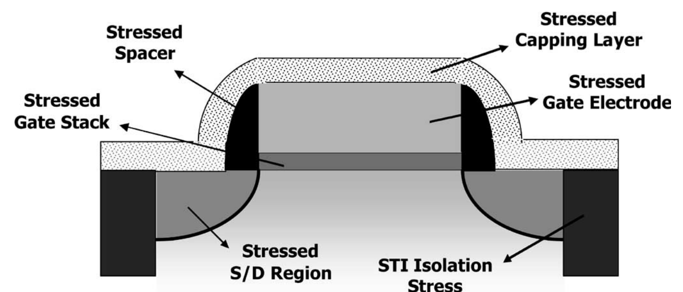

Fig. 1. Different ways in which stress can be introduced into the inversion layer in the bulk MOSFET.

First, a nonprocess-specific layout-dependent model for mobility enhancement through process-induced stress is described [10]. Mobility dependence on source/drain (S/D) length and channel length is captured through this model. The model is incorporated into the Berkeley short-channel insulated-gate FET model (BSIM) mobility model and verified against experimental data. Next, a dynamic behavior model for high-k transistors for capturing the fast transient charging effects is explained [11]. A subcircuit architecture of the model is developed to fit within a general compact model framework for the bulk MOSFET. Finally, efforts toward the modeling of multigate transistors are presented. Surface potential is calculated for a symmetric dependent double-gate MOSFET (DG-MOSFET) with finite body doping by solving the Poisson's equation using a perturbation approach. The drain–current of the DG-MOSFET is formulated in terms of the surface potential, and the model is compared against a two-dimensional (2-D) simulator for different body dopings and body thicknesses.

II. Mobility Model for Process-Induced Stress

Stress can be introduced into the inversion channel in different ways, as shown in Fig. 1. It is desirable to have a holistic mobility model that cannot only capture the effect of all the existing stress-inducing processes but also be able to model any future stress-inducing process. When silicon is stressed, the band structure is altered, and the effective mass of the carriers and the carrier scattering rates change. The resulting fractional change in resistivity is linearly proportional to the

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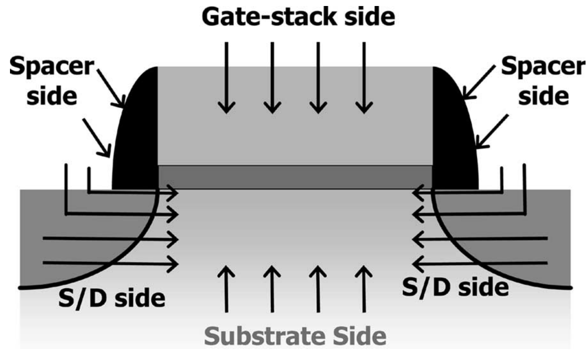

Fig. 2. Four distinct directions of stress transfer into the channel for any stress-inducing process.

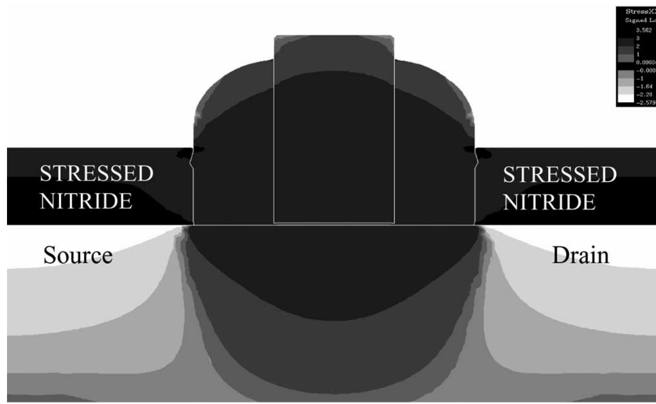

Fig. 3. Structure used to study the L dependence of the S/D-side stress transfer. The nitride layer with an intrinsic tensile stress of 1800 MPa is 75 nm thick. The tensile nitride layer transfers tensile stress to the channel.

local stress through the use of piezoresistive coefficients [12]. The nonlinearity in the change in resistivity is less than 2% for stresses of the order of 300 MPa [13]. After considering the nonuniformity of the stress in the inversion layer from source to drain, mobility enhancement is proportional to the average stress in the channel $S_{\rm AVG}(\mathcal{L})$, which is a function of the transistor layout $\mathcal{L}$, i.e.,

$$\frac{\Delta\mu}{\mu} \propto S_{\rm AVG}(\mathcal{L}). \tag{1}$$

Stress is transferred to the channel from four distinct directions, as shown in Fig. 2. It can be transferred from the S/D side, gate-stack side, spacer side, or substrate side. Substrate-side stress is mostly uniform through the channel and is simply modeled through a constant. Stress transfers from the other three directions are strongly layout dependent and are studied in detail using the TAURUS process simulator. Stress models are developed for each of these three directions independently and then combined to yield the complete layout-dependent holistic (nonprocess specific) mobility model.

S/D-side stress can originate due a stressor inside the S/D region (e.g., SiGe S/D process), adjacent to the S/D region (e.g., shallow trench isolation (STI) process), or on top of the S/D region (e.g., capping layer process). Fig. 3 shows the structure used to study the S/D-side stress-transfer component. A 75-nm-

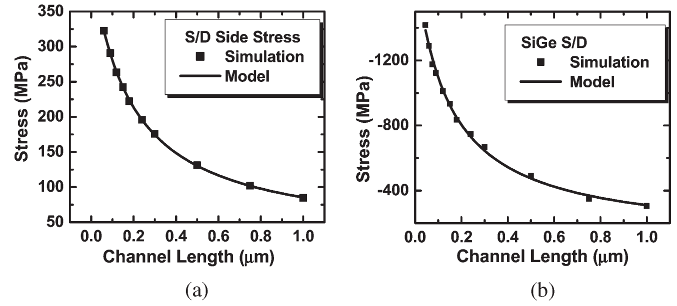

Fig. 4. Model fitting to the simulated average channel stress due to the S/D-side stress transfer for (a) a 75-nm-thick stressor on top of the S/D with an intrinsic tensile stress of 1800 MPa and (b) a 75-nm-thick SiGe layer inside the S/D region with 17% Ge concentration. As L increases, the average channel stress decreases in both cases.

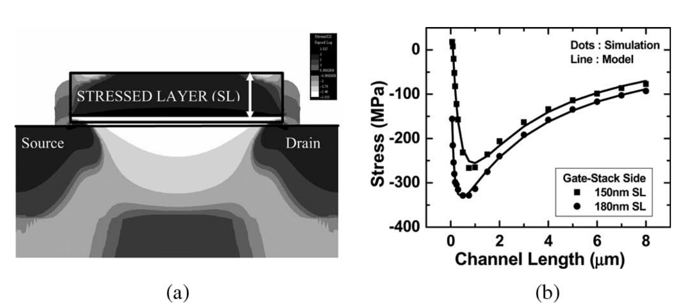

Fig. 5. Study of the gate-stack-side stress transfer. (a) Structure of the device used for the study. (b) Model fitting to the simulated average channel stress due to the gate-stack-side stress transfer. Note that the tensile stress in the stressed gate electrode transfers a compressive stress into the channel.

thick nitride layer with 1800-MPa intrinsic tensile stress is deposited on top of the S/D region as the stressor. The channel-length L dependence of the resulting average stress in the channel is captured through the following empirical model [Fig. 4(a)]:

$$S_{\rm AVG}(L) = A1 + \frac{A2}{A3 + L} \tag{2}$$

where $A1$ is the long-channel stress and $A2$ and $A3$ control the rate of change of stress with respect to channel length L. The same model is also able to capture the average channel stress for a SiGe structure, where the stressor is inside the S/D region [Fig. 4(b)], indicating that (2) can capture the L dependence of $S_{\rm AVG}$ for all kinds of S/D-side stressors. The values of $A1$, $A2$, and $A3$ are extracted separately for the different S/D-side stressors.

The source of stress transfer from the gate-stack side can be the stressed gate electrode, the stressed gate dielectric, or a stressed layer (SL) on top of the gate electrode. To analyze the gate-stack-side stress transfer, a gate electrode comprising of an SL and an unstressed poly-Si layer is used, as shown in Fig. 5(a). An intrinsic tensile stress of 1800 MPa is used for the SL. Fig. 5(b) shows the simulated average channel stress as a function of channel length for two different SL thicknesses. The amount of stressor is proportional to the channel length; hence, at a small L, the stress contribution to the channel is also small. As L increases, the amount of stressor increases,

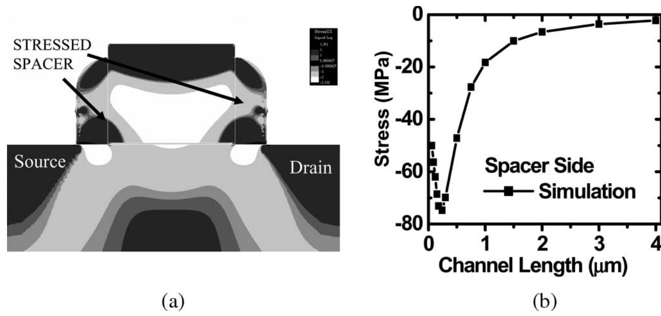

Fig. 6. Study of the spacer-side stress transfer. (a) Structure of the device used for the study. (b) Simulated average channel stress due to the spacer-side stress transfer.

and the stress increases, as shown in Fig. 5(b). However, at longer channel lengths, stress relaxation leads to a decrease in the stress. This trend can be captured through the following equation [Fig. 5(b)]:

$$S_{\mathrm{AVG}}(L) = B1 + \frac{B2}{B3 + L} - \frac{B4}{B5 + L} \tag{3}$$

where $B1$ is the long-channel stress and $B2{-}B5$ model the change of stress with respect to L at intermediate- and short-channel lengths.

The final component of stress transfer to the channel, the spacer-side stress transfer, can occur due to an SL outlining the spacer or the spacer having an intrinsic stress [Fig. 6(a)]. The resulting stress transfer has an L dependence similar to the gate-stack-side transfer [Fig. 6(b)]. However, since the process simulations showed that the stress transfer to the channel from the spacer side is very small, this component is neglected.

In a similar vein, the S/D length L_{SD} can be varied, and the model for average channel stress as a function of L_{SD} can be written as [10]

$$S_{\mathrm{AVG}}(L_{\mathrm{SD}}) = C1 - \frac{C2}{C3 + L_{\mathrm{SD}}} \tag{4}$$

where $C1$, $C2$, and $C3$ are the fitting parameters.

Using (1)–(4), the holistic model for mobility enhancement through process-induced stress as a function of channel length and S/D length can be written as

$$\mu = \mu_0 \cdot \left(1 + E1 + \frac{E2}{E3 + L} - \frac{E4}{E5 + L}\right) \cdot \left(1 + E6 + \frac{E7}{E8 + L_{\mathrm{SD}}}\right) \tag{5}$$

where μ_0 is the mobility model with no stress, $E1$–$E5$ model the L dependence in (2) and (3), and $E6$–$E8$ control the L_{SD} dependence in (4). This model is added to the BSIM4 mobility model for verification against experimental data. In order to extract the model parameters, an array of transistors with different channel lengths L and different S/D lengths L_{SD} is needed. The parameters of the stress model, along with the complete mobility model parameters, are extracted through a global fitting to the drain–current in the linear regime for the aforementioned array of test structures.

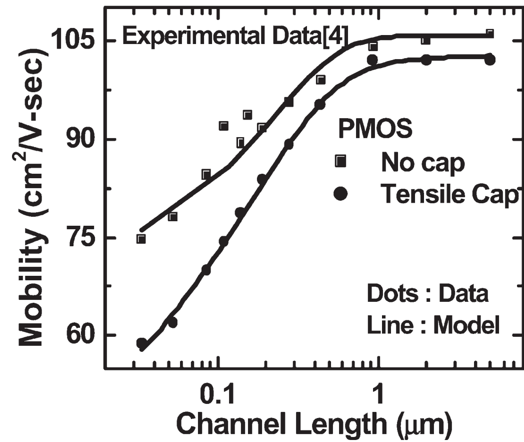

Fig. 7. Experimental verification of the holistic mobility model for a capping layer process. Experimental data is obtained from [4].

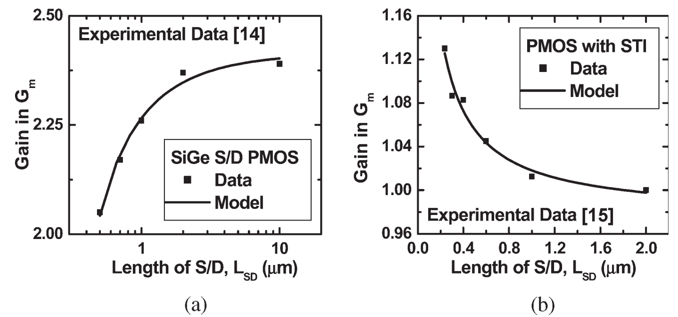

Fig. 8. Experimental verification of the holistic mobility model for S/D-length dependence for (a) the SiGe S/D process (data from [14]) and (b) the STI process (data from [15]).

The capping layer process is the best test case since it has stress transfers from all three directions. Reduction in hole mobility as a function of channel length is reported in [4] for a tensile capping layer process. The BSIM4 mobility model is first fit to the control wafer mobility. The holistic stress model is then added to capture the change in hole mobility due to the capping layer. Fig. 7 shows the excellent fit of the complete model to the experimental data. Fig. 8 shows the verification of the L_{SD} dependence in the model against experimental data for both SiGe S/D and STI processes.

III. Dynamic Behavior Model for High-k MOSFET

High-k transistors exhibit dynamic behavior such as threshold-voltage V_{th} instability and hysteresis in the drain–current [16], [17] due to charging/discharging of the traps in the high-k gate stack [18], [19]. The change in V_{th} of the device is proportional to the filled trap density n_{tr}, i.e.,

$$\Delta V_{\mathrm{th}} \propto n_{\mathrm{tr}}(t). \tag{6}$$

Charging/discharging of the traps can occur through one of the following: Mechanism-direct tunneling to the trap, gate current flowing through the gate stack, or indirect tunneling from interfacial traps. The kinetics of trap filling in all these cases can be modeled through Shockley–Read–Hall (SRH)

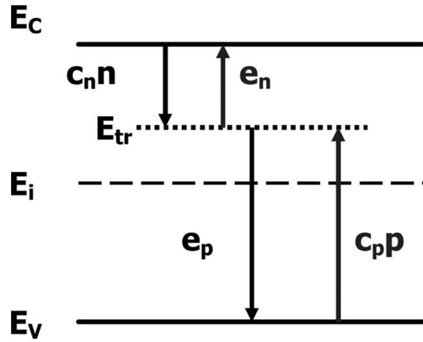

Fig. 9. SRH trap/detrap mechanism (E_{tr} is the energy level of the trap).

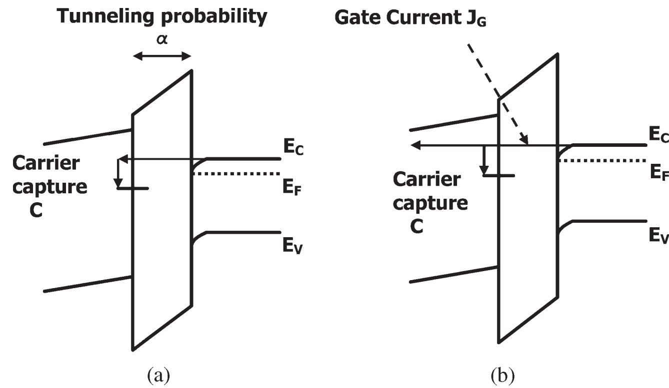

Fig. 10. Trap filling through (a) direct tunneling and (b) gate current mechanisms.

statistics (Fig. 9). Under moderate and strong inversion, the rate equation can be expressed as (for nMOSFETs)

$$\frac{dn_{\mathrm{tr}}}{dt} = c_n n(N_{\mathrm{tr}} - n_{\mathrm{tr}}) - e_n n_{\mathrm{tr}} \tag{7}$$

where N_{tr} is the available trap density, n is the electron density, and c_n and e_n denote the electron capture and emission constants, respectively. Since the rate of change of filled traps at equilibrium is zero, one can rewrite (7) as [11]

$$\frac{dn_{\mathrm{tr}}}{dt} = c_n n\left(N_{\mathrm{tr}} - (1 + A) \cdot n_{\mathrm{tr}}\right) \tag{8}$$

where $A = ((E_{\mathrm{tr}} - E_F)/kT)$.

Equation (8) is the characteristic equation that controls the density of filled traps as a function of time. The exact expression of capture constant c_n is trapping process dependent. However, as will be explained, the functional form of c_n remains essentially the same for all of the mentioned trapping/detrapping mechanisms.

Fig. 10(a) shows trapping through direct tunneling as a two-step process wherein the carriers tunnel through the gate stack to the trap site with a tunneling probability α and are captured with a probability C. Employing Wentzel–Kramers–Brillouin (WKB) approximation to evaluate α, one can show that

$$c_n = C \cdot e^{fn(-t_{\mathrm{oxp}}, V_{\mathrm{ox}})} \tag{9}$$

where t_{oxp} is the physical thickness of the high-k dielectric and V_{ox} is the voltage drop across it. If the gate current is the dominant source of carriers, α is proportional to the gate current, which in turn has the same functional form as (9). Indirect tunneling of carriers from interfacial traps will also have a similar exponential dependence through the tunneling probability term.

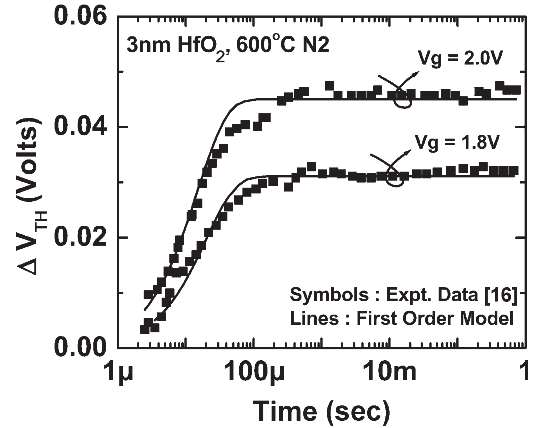

Fig. 11. Verification of the first-order approximation of the rate equation for smaller V_{th} shifts. Experimental data is obtained from [16].

For the rate equation (8) to work under a generalized situation with several traps at different energy levels and different spatial locations, introduce fitting parameters $A1$, $A2$, $C1$, $C2$, $C3$, and $C4$, i.e.,

$$A = A1 \cdot V_g + A2 \cdot V_g^2 \tag{10}$$

$$c_n \cdot n = C1 \cdot (1 + C2 \cdot V_{\mathrm{ox}}) \cdot e^{-t_{\mathrm{oxp}}\left(-C3 \cdot V_{\mathrm{ox}} - C4 \cdot V_{\mathrm{ox}}^2\right)}. \tag{11}$$

A pulse measurement methodology is used to extract the model parameters [16], [17]. A voltage pulse is applied to the gate of the high-k transistor, and the transient drain–current is measured. The reduction in drain–current with time is used to calculate the corresponding V_{th} shift. The model parameters are then extracted by a global fitting to the observed V_{th} shift for different gate pulse magnitudes.

The model is verified against the experimentally measured V_{th} shifts. For small V_{th} shifts, since the capture constant c_n and carrier density n are nearly constant with time, the rate equation is a simple first-order differential equation whose solution is given by

$$n_{\mathrm{tr}}(t) = \frac{N_{\mathrm{tr}}}{1 + A} \cdot \left(1 - e^{-(1+A)c_n n t}\right). \tag{12}$$

Fig. 11 shows that the first-order model agrees well with small V_{th} shifts. However, in case of larger V_{th} shifts, the c_n and n in (8) vary with time, and the rate equation is a highly nonlinear differential equation. The rate equation can be implemented as a subcircuit (Fig. 12) in the BSIM4 framework with the addition of two nodes. In the subcircuit (Fig. 12), the voltage at the node V_{out}, which is $n_{\mathrm{tr}}(t)$, can be expressed in terms of the circuit elements as

$$C \frac{dn_{\mathrm{tr}}(t)}{dt} = \frac{N_{\mathrm{tr}} - n_{\mathrm{tr}}(t)}{R_1} - \frac{n_{\mathrm{tr}}(t)}{R_2}. \tag{13}$$

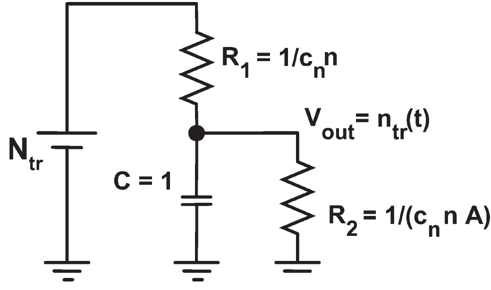

Fig. 12. Subcircuit to implement the nonlinear differential equation that models the high-k dynamic behavior in a general compact model framework. R_1 controls the trapping rate, and R_2 controls the detrapping rate. Two additional nodes are added to the MOSFET model due to the subcircuit.

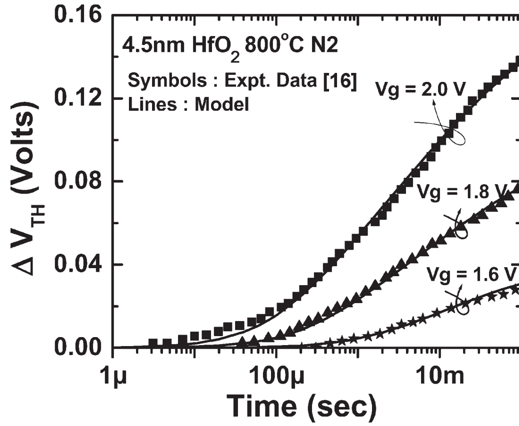

Fig. 13. Verification of the model for larger V_{th} shifts. Experimental data is obtained from [16].

Using $C = 1$ and the values of R_1 and R_2 defined in Fig. 12, (13) is exactly identical to the rate equation (8). The subcircuit is solved in parallel with the core BSIM4 model, and the node voltage $n_{\mathrm{tr}}(t)$ is used to dynamically correct the V_{th} of the transistor though the following:

$$V_{\mathrm{th}} = V_{\mathrm{th0}} - \frac{qn_{\mathrm{tr}}(t)}{C_{\mathrm{ox}}} \tag{14}$$

where V_{th0} is the threshold voltage calculated by the core MOSFET model and C_{ox} is the gate capacitance. This subcircuit approach can be used to implement the model in any bulk MOSFET compact model. Fig. 13 shows that the complete model can also fit experimentally measured larger V_{th} shifts.

IV. Multigate Model

An analytical surface-potential-based model has been developed for the symmetric dependent DG-FET with finite body doping. The word "symmetric" refers to the physical symmetry in structure, and "dependent" implies that the front gate and back gate have the same potential. The one-dimensional (1-D) Poisson's equation including both inversion carriers and bulk charge in the body can be written as

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\epsilon_{\mathrm{Si}}} \cdot \left(e^{\frac{q\psi}{kT}} \cdot e^{\frac{-q\phi_B}{kT}} \cdot e^{\frac{-qV_{\mathrm{ch}}}{kT}} + e^{\frac{q\phi_B}{kT}}\right) \tag{15}$$

where $\psi(x)$ is the electronic potential in the body, $\phi_B = (kT/q)ln(N_A/n_i)$, V_{ch} is the channel potential, and N_A is the body doping. The Poisson's equation is solved by the use of perturbation approach. Under the perturbation approach, the body-charge term in (15) is neglected first, and the surface potential only due to the inversion-carriers term is calculated $(\psi_1(x))$. The perturbation in $\psi(x)$ due to the body doping $\psi_2(x)$ is then calculated by substituting

$$\psi(x) = \psi_1(x) + \psi_2(x) \tag{16}$$

in (15) and using the value of $\psi_1(x)$. This method yields the solution in both the fully depleted and partially depleted regimes of transistor operation.

In the fully depleted regime, the contribution of inversion carriers to the surface potential ψ_{inv} can be derived by neglecting the bulk-charge term in (15) and integrating it twice [20] such that

$$\begin{aligned}\psi_{\mathrm{inv}} &= \psi_1|_{x=-\frac{T_{\mathrm{Si}}}{2}} \\ &= \psi_0 - \frac{2kT}{q}\ln\left(\cos\left(\sqrt{\frac{q^2}{2\epsilon_{\mathrm{Si}}kT}\frac{n_i^2}{N_A}e^{\frac{-qV_{\mathrm{ch}}}{kT}}}e^{\frac{q\psi_0}{2kT}}\frac{T_{\mathrm{Si}}}{2}\right)\right)\end{aligned} \tag{17}$$

where ψ_0 is the potential at the center of the body, i.e., $\psi_0 = \psi_1(0)$, and T_{Si} is the body thickness. Since the contribution of bulk charge to the potential and electric field at midplane is zero, $d\psi_2/dx|_{x=0} = 0$, and $\psi_2|_{x=0} = 0$. Substituting (16) in (15) and using the aforementioned boundary conditions, the correction to surface potential due to bulk charge $\psi_c = \psi_2|_{x=-(T_{\mathrm{Si}}/2)}$ can be derived as

$$\psi_c = \frac{2qn_i}{\epsilon_{\mathrm{Si}}} \cdot \frac{e^{\frac{q\phi_B}{kT}}}{a}\left(\frac{e^{T_{\mathrm{Si}}\frac{\sqrt{a}}{2}} - 1}{2e^{\frac{T_{\mathrm{Si}}}{2}\frac{\sqrt{a}}{2}}}\right)^2,$$
$$\text{where} \quad a = \frac{q^2 n_i}{\epsilon_{\mathrm{Si}}kT} \cdot e^{\frac{q(\psi_{\mathrm{inv}} - V_{\mathrm{ch}} - \phi_B)}{kT}}. \tag{18}$$

The electric field at the surface can be easily obtained by integrating (15) once. Gauss law is shown at the bottom of the page where $\psi_s = \psi_{\mathrm{inv}} + \psi_c$. The surface potential ψ_s in the fully depleted regime is determined by solving (17)–(21) simultaneously.

$$V_g = V_{\mathrm{FB}} + \psi_s + \frac{\epsilon_{\mathrm{Si}}}{C_{\mathrm{ox}}}\sqrt{\frac{2qn_i}{\epsilon_{\mathrm{Si}}} \cdot \left(\frac{e^{\frac{q\psi_s}{kT}} - e^{\frac{q\psi_o}{kT}}}{q/kT} \cdot e^{\frac{-q\phi_B}{kT}} \cdot e^{\frac{-qV_{\mathrm{ch}}}{kT}} + e^{\frac{q\phi_B}{kT}} \cdot (\psi_s - \psi_o)\right)} \tag{19}$$

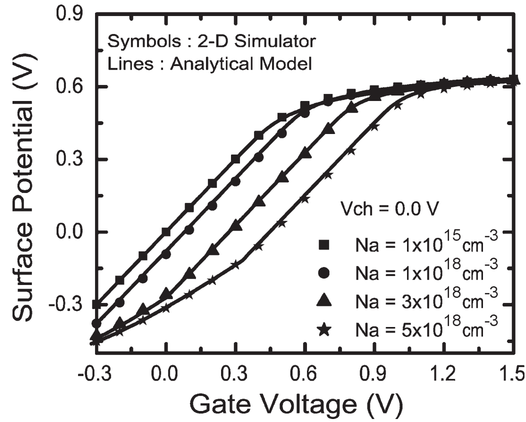

Fig. 14. Surface potential ψ_s for the case of $V_{\mathrm{ch}} = 0$ V referenced to TAURUS. The analytical model agrees with 2-D simulator for both lightly doped and heavily doped DG-MOSFETs.

In the partially depleted regime, the depletion width is bias dependent. At the edge of the depletion width x_{dep}, the electronic potential is zero; hence, $\psi_1|_{x=x_{\mathrm{dep}}} = 0$. With the aforementioned changes, ψ_{inv} and ψ_c can be rederived for the partially depleted regime similar to the fully depleted regime. ψ_{inv} can be expressed as

$$\begin{aligned}\psi_{\mathrm{inv}} &= \psi_1|_{x=-\frac{T_{\mathrm{Si}}}{2}} \\ &= -\frac{2kT}{q}\ln\left(\cos\left(\sqrt{\frac{q^2}{2\epsilon_{\mathrm{Si}}kT}\frac{n_i^2}{N_A}e^{\frac{-qV_{\mathrm{ch}}}{kT}}}\cdot x_{\mathrm{dep}}\right)\right) \qquad (20)\end{aligned}$$

where x_{dep} is the bias-dependent depletion width. The correction term in the surface potential due to bulk charge ψ_c can be expressed as

$$\begin{aligned}\psi_c &= \frac{2qn_i}{\epsilon_{\mathrm{Si}}}\cdot\frac{e^{\frac{q\phi_B}{kT}}}{a}\left(\frac{e^{x_{\mathrm{dep}}\sqrt{a}}-1}{2e^{x_{\mathrm{dep}}\frac{\sqrt{a}}{2}}}\right)^2, \\ \text{where}\quad a &= \frac{q^2 n_i}{\epsilon_{\mathrm{Si}}kT}\cdot e^{\frac{q(\psi_{\mathrm{inv}}-V_{\mathrm{ch}}-\phi_B)}{kT}}. \qquad (21)\end{aligned}$$

Gauss law in the partially depleted regime is shown at the bottom of the page. Surface potential ψ_s in the partially depleted regime is obtained by solving (20)–(22) simultaneously. The unknown variable x_{dep} in the solution of the partially depleted regime replaces the unknown ψ_0 in the solution of the fully depleted regime.

Fig. 14 shows that the surface potential ψ_s calculation from the model agrees well with 2-D simulations for a DG-MOSFET with finite body doping in both the partially depleted regime and the fully depleted regime. Typical device parameters used for simulations are $T_{\mathrm{ox}} = 2$ nm, $T_{\mathrm{Si}} = 20$ nm, and $L = 1$ μm, unless otherwise specified. Using charge-sheet approximation [21] and assuming a fully depleted body, the drain–current can be formulated as

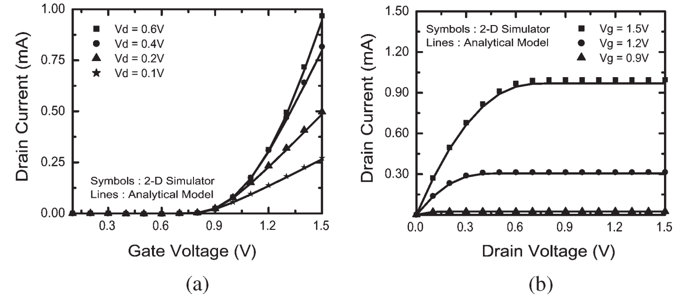

Fig. 15. Drain–current of a DG-MOSFET with a body doping of 3×10^{18} cm^{-3}, $T_{\mathrm{ox}} = 2$ nm, and $L = 1$ μm. (a) I_d–V_g characteristics. (b) I_d–V_d characteristics. The constant mobility model is used in the device simulations and the analytical model.

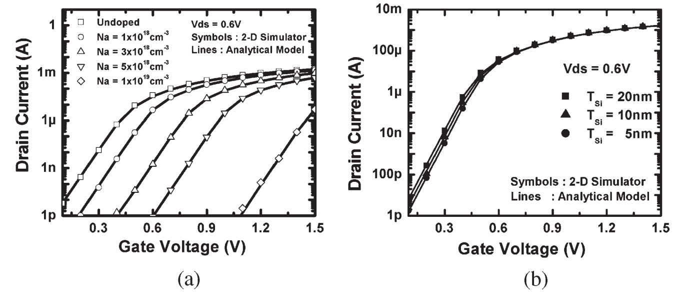

Fig. 16. Comparison of drain–current between the analytical model and the 2-D device simulator for (a) different body dopings N_A and (b) different body thicknesses T_{Si}. For all cases, $L = 1$ μm, and $T_{\mathrm{ox}} = 2$ nm.

$$\begin{aligned}I_d = 2\mu C_{\mathrm{ox}}\frac{W}{L}&\left(V_g - V_{\mathrm{fb}} - \frac{\psi_{\mathrm{ss}}+\psi_{\mathrm{sd}}}{2} - \frac{qN_AT_{\mathrm{Si}}}{2C_{\mathrm{ox}}} + \frac{kT}{q}\right) \\ &\times(\psi_{\mathrm{sd}}-\psi_{\mathrm{ss}}) \qquad (23)\end{aligned}$$

where ψ_{ss} and ψ_{sd} are the surface potentials at the source and drain, respectively. The solution of (17)–(22) yields the surface potential at the source end ψ_{ss} when $V_{\mathrm{ch}} = 0$. The surface potential at the drain end ψ_{sd} is evaluated by solving (17)–(22) when $V_{\mathrm{ch}} = V_{\mathrm{ds}}$, where V_{ds} is the potential difference between the drain and source terminals. The factor of 2 in (23) accounts for the two inversion channels. The model can predict the drain–current very accurately for a DG-MOSFET with finite body doping, as shown in Fig. 15. The model is also able to predict the drain–current dependence on body doping and body thickness very accurately, as shown in Fig. 16, without the use of any fitting parameters. Since volume inversion was captured through surface potential calculation, the I–V model also shows volume inversion.

$$V_g = V_{\mathrm{FB}} + \psi_s + \frac{\epsilon_{\mathrm{Si}}}{C_{\mathrm{ox}}}\sqrt{\frac{2qn_i}{\epsilon_{\mathrm{Si}}}\cdot\left(\frac{e^{\frac{q\psi_s}{kT}}-1}{q/kT}\cdot e^{\frac{-q\phi_B}{kT}}\cdot e^{\frac{-qV_{\mathrm{ch}}}{kT}} + e^{\frac{q\phi_B}{kT}}\cdot\psi_s\right)} \qquad (22)$$

V. Conclusion

BSIM models and other compact models for MOSFETs are being continuously improved in parallel with technology advancements to enable an efficient and rapid adoption of new technologies. Improvements to the bulk MOSFET model by modeling new effects and new materials have been presented. These improvements can be adopted in any bulk MOSFET compact model. The change in carrier mobility due to process-induced stress has been modeled for bulk MOSFETs. The model is nonprocess specific and can handle channel-length and S/D-length dependence. A new model to capture the dynamic behavior in high-k transistors has been developed. The model can be incorporated into a bulk MOSFET compact model framework through the addition of a subcircuit that introduces two new nodes into the bulk model. Finally, a new analytical model for a symmetric DG-MOSFET with finite body doping has been developed. Surface potential is calculated using a perturbation approach. A surface-potential-based drain–current model is derived and demonstrated to agree very well with 2-D simulations for different body dopings and body thicknesses without the use of any fitting parameters.

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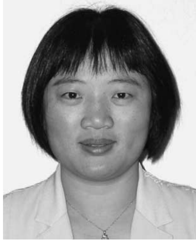

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