

CMOS compatible transformer power combiner

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A new approach for power combining several low-voltage CMOS amplifiers using a new on-chip transformer architecture is presented. The transformer utilises lateral coupling and thus the layout only requires one relatively thick metal layer. Full-wave electromagnetic simulation confirms the operation and low insertion loss of the transformer.

Introduction: Power amplifiers are a key building block in any radio transceiver, usually necessitating a multi-chip module solution owing to the requirement of a specialised process with high voltage breakdown and low-loss passive components. Several researches have demonstrated that CMOS technology is a viable option for implementation of the power amplifier. Fully integrated transformer based power combining has been demonstrated by [1], utilising so-called ‘slab’ inductors to realise highly efficient on-chip magnetic coupling structures called the DAT. In this Letter we propose a classic transformer based power combiner, shown in Fig. 1. Each pair of windings are realised with ring based transformer structures that are simple to design and scale with frequency. Since each stage is DC isolated, each amplifier runs on a low supply voltage, allowing low breakdown transistors to be employed. An additional benefit of the ring based structure is simple power control. Since each stage operates independently, we can turn off amplifier stages to back-off power without dramatically altering the efficiency of the power combiner [2].

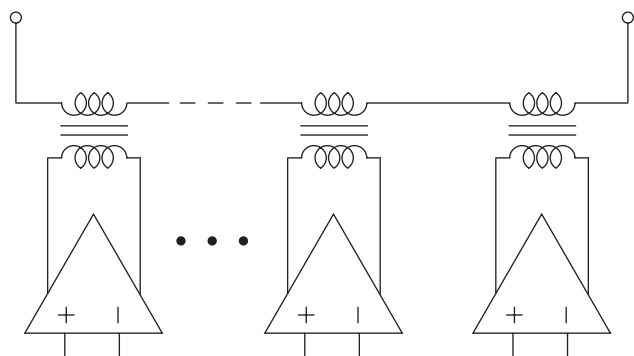


Fig. 1 Simple transformer based power combining; allows low-voltage stages to sum power into load efficiently [1]

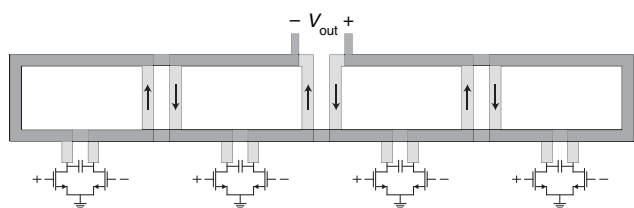


Fig. 2 Layout of power combiner using vertical transformer structure

Proposed transformer: One of the primary advantages of the DAT is the creation of virtual grounds which eliminate the need for inductor leads, virtually turning ‘slabs’ of metal into inductors [1]. As shown in Fig. 2, in a simple transformer layout, the adjacent windings have current in opposite direction, and thus do not contribute as much flux and coupling to the secondary. One approach to minimise the internal flux cancellation is to space the windings as far apart as possible and utilise an oval winding, as shown in Fig. 3a. At the expense of space this is an effective approach and a high efficiency dual-layer structure has been demonstrated [2]. With only a single thick metal layer, a lateral coupling structure, shown in Fig. 3b, is a good approach but has some shortcomings. One major shortcoming is current crowding at the inner conductor edges, which results from the proximity effect, which increases the resistance of the structure.

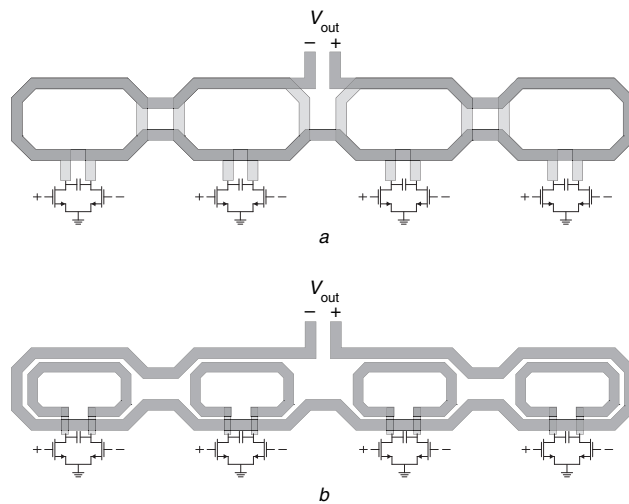


Fig. 3 Modified vertically coupled and laterally coupled transformer structures

a Modified vertically coupled transformer structure
b Laterally coupled transformer structure

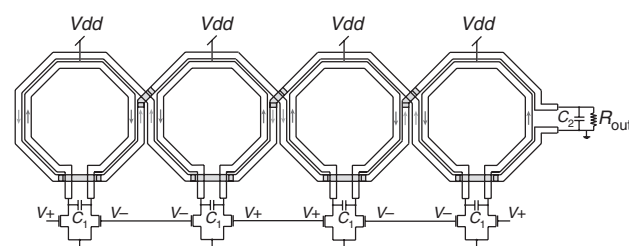


Fig. 4 Proposed ‘figure 8’ transformer layout

A new ‘figure 8’ style layout is proposed and shown in Fig. 4. Note that each individual amplifier drives a single loop inductor but the secondary is implemented in alternating orientation. This layout minimises the effects of the internal flux cancellation discussed and creates convenient locations for the transistor to connect to the primary loops, minimising extraneous lead inductance. An additional benefit arises from the alternating direction of the secondary windings. As a result, the secondary loop is immune to a common-mode coupling from a distant source since the incoming magnetic flux induces voltages of opposite polarity across each ‘figure 8’ section. It is thus wise to employ an even number of stages.

In the layout of the amplifier it is convenient to place a ground ring around the inductor to provide low inductance paths to supply rails for the amplifier bypass capacitors. This loop unfortunately lowers the quality factor of the transformer owing to induced eddy currents. The eddy currents arise from the magnetic leakage due to the imperfect coupling between the secondary and primary loops. Since the secondary loop is physically larger, its magnetic flux is not completely cancelled by the smaller inner loops. By alternating the orientation of the secondary loops, though, as in the ‘figure 8’, the eddy currents are suppressed substantially, allowing a more practical layout to be realised.

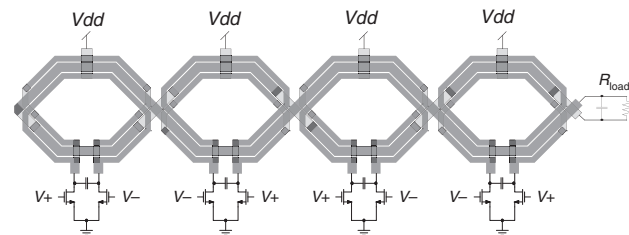


Fig. 5 Modified symmetric coupling ‘figure 8’ transformer layout

An additional improvement to the layout is shown in Fig. 5. A second primary winding has been added, so now coupling to the secondary occurs from an inner and outer loop. The parallel turn lowers the resistance of the winding in an important way since at high frequency

the current crowds to the edges of the conductors. Because of the proximity effect, in the single winding case the edge coupled to the secondary takes the bulk of the current. With a two winding approach, both edges now contribute to coupling and to current flow, cutting the loss substantially.

Simulation results: Full-wave electromagnetic simulation is used to predict the high frequency performance of the inductor loops. Previous experience has confirmed the validity of the simulations, as the performance of a fully integrated four-stage vertically coupled transformer structure was predicted and verified against measurements [2]. In this work we used the same tools and simulation setup, including Agilent Momentum and Ansoft HFSS. The simulation of several prototype transformers was performed to realise a 5 GHz power combiner for WLAN applications. The back-end of a 90 nm CMOS process was used in the simulations, which is very typical of a modern CMOS digital process. Only the top metal layer was employed for the windings while underpass elements were realised with the lower metal layers.

The best achievable performance for the power combiner is an insertion loss of 1.35 dB (75%), shown in Fig. 6. The insertion loss varies by only 0.4% over the band of interest. The performance of this transformer compares favourably with our previous experience with a dual-thick metal layer RF CMOS process where the optimised transformer achieved an efficiency of 0.97 dB (80%) [2]. Other researchers have reported the simulated performance of power combiners and comparison with these works is presented in Table 1. The proposed transformer is one the smallest reported, 0.65×0.15 mm, even compared to a 20 GHz combiner [3]. While the efficiency is not as great, it should be noted that no special process options were employed (such as gold metal in [4] or thick metal layers in the other works).

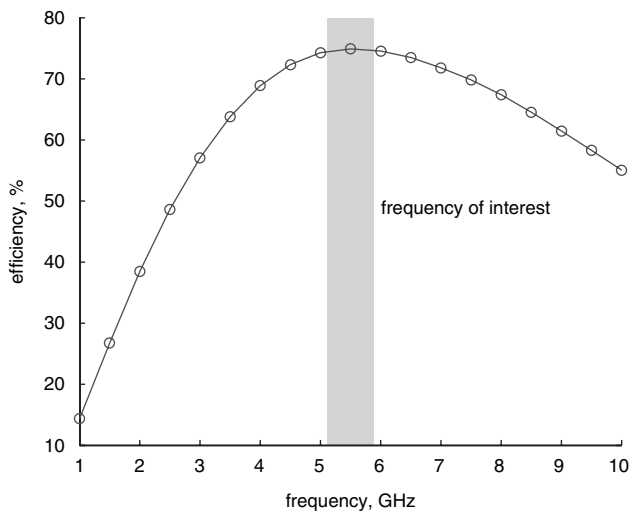


Fig. 6 Transformer efficiency against frequency

Table 1: Comparison between state-of-the-art power combining networks

Process	Type	Frequency (GHz)	η (%)	Size (mm ²)	Ref.
0.35 μ m BiCMOS	Slab	2.4	70.5	0.8×0.8	[1]
0.18 μ m CMOS	Slab	2.4	83	0.8×0.5	[5]
RF GaAs	Slab	2	87.7	1.2×1.2	[4]
RF 0.20 μ m SiGe	Slab	21–26	77.6	0.4×0.2	[3]
RF 0.13 μ m CMOS	Loop	2.4	80	1.5×0.25	[2]
0.09 μ m CMOS	Loop	5.35	75	0.65×0.15	This work

Conclusion: By utilising a new ‘figure 8’ dual loop transformer, a structure compatible with standard digital CMOS process, we have demonstrated an efficient and compact layout for a power combiner. The power combiner allows full integration of matching and combining networks on the CMOS die, which has the potential to dramatically lower the cost of a PA. The efficiency is comparable to other reported structures utilising specialised process options.

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References

- 1 Aoki, I., *et al.*: ‘Distributed active transformer—a new power-combining and impedance-transformation technique’, *IEEE Trans. Microw. Theory Tech.*, 2002, **50**, pp. 316–331
- 2 Liu, G., King, T.-J., and Niknejad, A.M.: ‘A 1.2 V, 2.4 GHz fully integrated linear CMOS power amplifier with efficiency enhancement’. To be presented in Proc. of IEEE Custom Integrated Circuits Conference, 2006
- 3 Cheung, T.S.D., and Long, J.R.: ‘A 21–26-GHz SiGe bipolar power amplifier MMIC’, *IEEE J. Solid-State Circuits*, 2005, **40**, pp. 2583–2597
- 4 Kim, S., *et al.*: ‘An optimized design of distributed active transformer’, *IEEE J. Microw. Theory Tech.*, 2005, **53**, pp. 380–388
- 5 Kang, J., Hajimiri, A., and Kim, B.: ‘A single-chip linear CMOS power amplifier for 2.4 GHz WLAN’. Proc. ISSCC, 2006