

9.6/4.8 GHz dual-mode voltage-controlled oscillator with injection locking

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A prototype dual-mode voltage-controlled oscillator supporting two simultaneous oscillation modes is fabricated and demonstrated in a 0.18 μm CMOS process. The oscillator has two resonant ports while sharing one bias. Injection locking is applied to lock the low frequency, 4.8 GHz, to half of the high frequency, 9.6 GHz. The oscillator core consumes 7 mA from a 1.8 V supply. Measurement shows a tuning range of 5% and phase noise is -103 and -109 dBc/Hz measured at 1 MHz offset from the high and low frequency tones, respectively.

Introduction: Power consumption in a phase-locked loop frequency synthesiser increases as the frequency becomes higher and higher. Applying novel blocks which integrate multiple functions in the conventional topology is an efficient way to reduce power consumption. In this Letter, a dual-mode voltage-controlled oscillator (DMVCO) with injection locking is demonstrated to combine the functionalities of a conventional voltage-controlled oscillator (VCO) and an injection-locked divider. Multimode oscillation can be generated from a high-order network [1–3], and it has more complex and potentially beneficial dynamic characteristics compared to a conventional second-order network. We present both network design and circuit design issues in DMVCO.

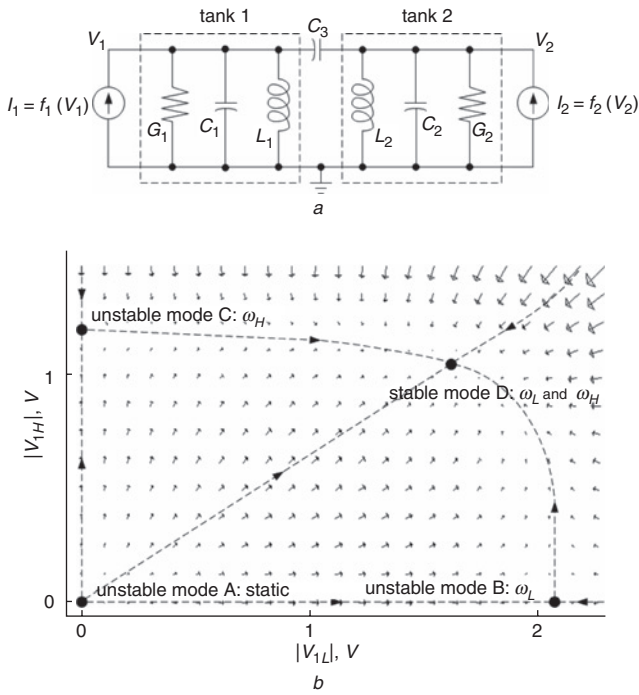


Fig. 1 Oscillator based on capacitively-coupled parallel LC tank, and phase portrait for oscillator

a Oscillator
b Phase portrait

Dual-mode oscillation study: Consider the fourth-order LC network in Fig. 1a. To find resonant frequencies of the network, the two port Y matrix is calculated, where all memoryless components are neglected under a high quality factor assumption

$$M_Y = \begin{bmatrix} j\omega(C_1 + C_3) + \frac{1}{j\omega L_1} & -j\omega C_3 \\ -j\omega C_3 & j\omega(C_2 + C_3) + \frac{1}{j\omega L_2} \end{bmatrix} \quad (1)$$

$$\det(M_Y) = 0 \quad (2)$$

By solving (2) for ω , the two resonant frequencies can be listed in (3a–b):

$$\omega_L = \sqrt{\frac{\left(\frac{((C_3/L_1) + (C_3/L_2) + (C_1/L_2) + (C_2/L_1))}{\sqrt{((C_3/L_1) - (C_3/L_2) - (C_1/L_2) + (C_2/L_1))^2 + (4 \times C_3^2)/(L_1 \times L_2)}} \right)}{2 \times (C_3 \times C_1 + C_3 \times C_2 + C_1 \times C_2)}} \quad (3a)$$

$$\omega_H = \sqrt{\frac{\left(\frac{((C_3/L_1) + (C_3/L_2) + (C_1/L_2) + (C_2/L_1))}{\sqrt{((C_3/L_1) - (C_3/L_2) - (C_1/L_2) + (C_2/L_1))^2 + (4 \times C_3^2)/(L_1 \times L_2)}} \right)}{2 \times (C_3 \times C_1 + C_3 \times C_2 + C_1 \times C_2)}} \quad (3b)$$

In a general case, the two frequency components exist simultaneously at both ports so that the voltage at each port can be written as (4a–b) by ignoring their harmonics:

$$V_1 = V_{1H} \cos(\omega_H t + \theta_{1H}) + V_{1L} \cos(\omega_L t + \theta_{1L}) \quad (4a)$$

$$V_2 = V_{2H} \cos(\omega_H t + \theta_{2H}) + V_{2L} \cos(\omega_L t + \theta_{2L}) \quad (4b)$$

Since (2) is satisfied, $|V_{1H}|$ and $|V_{2H}|$ are linearly correlated, and so are $|V_{1L}|$ and $|V_{2L}|$. Therefore, a 2-D phase portrait about $|V_{1H}|$ and $|V_{1L}|$, shown in Fig. 1b, can describe the oscillation amplitude dynamics if the amplitude variation is much slower than the oscillation frequencies ω_H and ω_L . Each arrow in the plot represents the state transition velocity at that point. There can be at most four possible stable states. To utilise the dual resonant frequencies, a stable state D is desired while other states need to be unstable. Fig. 1b gives an example of the desired case. It can be read from the plot that the oscillator will eventually converge to stable dual-mode oscillation regardless of its initial state. In addition to stability, stable oscillation voltage amplitudes can be predicted from this phase portrait.

DMVCO circuit design: A complete schematic diagram of the proposed DMVCO is shown in Fig. 2. The differential capacitive-coupled LC tank used in the schematic diagram, which resonances at about 10 and 5 GHz, is basically a differential extension of the single-ended structure in Fig. 1a with two additional characteristics. First, C_1 and C_2 are tunable capacitors controlled by the same tuning signal. Secondly, the centre taps of the on chip spiral inductors L_1 and L_2 are connected and used as a DC bias current path so that the two cross-coupled pairs can share the same DC bias current. Aside from a conventional second-order network, nonlinear functions presented at terminals will affect the oscillation amplitude phase portrait. The cross-coupled pair must be sized carefully, usually by sweeping different size combinations, to ensure the dual-mode oscillation state is stable and other states are unstable over the whole frequency tuning range.

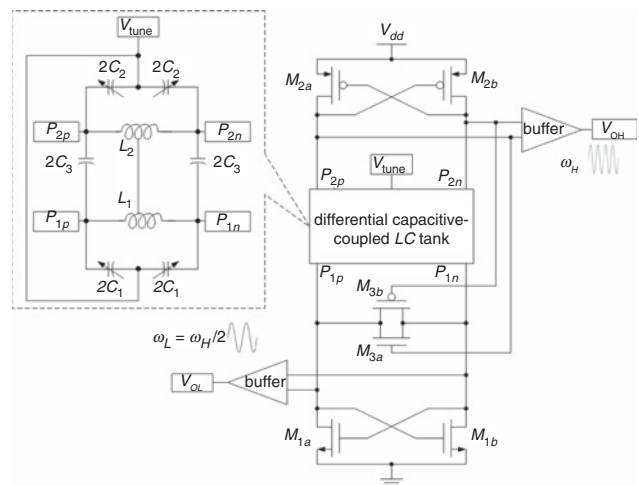


Fig. 2 Schematic diagram of DMVCO

Injection locking technique [4] is applied to entrain the low frequency to half of the high frequency. A periodically on-and-off switch, M_{3a} and M_{3b} , driven by the signal from port 2 is presented at port 1. The locking range analysis is based on [5]. Coexistence of both

fundamental and second harmonic at the gate and drain of the switch helps to enhance the locking range.

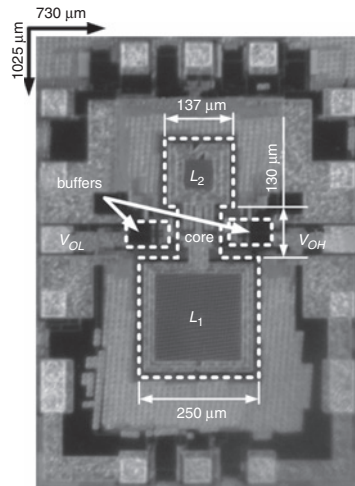


Fig. 3 Die photo of DMVCO

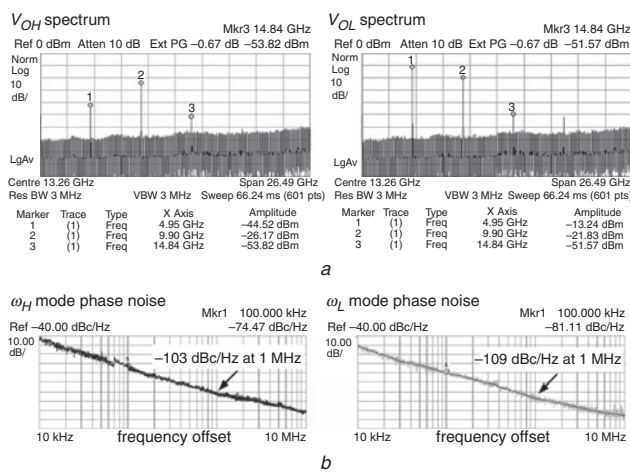


Fig. 4 Output voltage spectra of two ports, and phase noise of two oscillation tones

a Output voltage spectra
b Phase noise

Measurement: The DMVCO is implemented in a 0.18 μm CMOS process. The die photo is shown in Fig. 3. The DMVCO core consumes 7 mA from a 1.8 V supply. The spectra of the two outputs are shown in Fig. 4a. Dual-mode oscillations are present at each port with one primary mode and one secondary mode. The

measured primary tone amplitudes are $|V_{1L}|_{meas} = -13$ dBm and $|V_{2H}|_{meas} = -26$ dBm. Since each buffer has a gain of -23 dB at both frequencies, and the SMA cable used in measurement attenuates the signal by approximately 2 dB, the output signals directly from the DMVCO are $|V_{1L}|_{core} \approx 12$ dBm and $|V_{2H}|_{core} \approx -1$ dBm. The locking range of the oscillation frequency is 5%, from 9.40 to 9.92 GHz. Both the relatively low $|V_{2H}|_{core}$ and limited tuning ranges result from errors in estimation of the layout parasitic, especially the inductor L_2 . The stable dual-mode oscillation state shifts from its expected position and the two resonant frequencies are not perfectly aligned. Once the two inductor values, or more importantly the ratio of their values, are calibrated in the design, a DMVCO design will not be more sensitive to process variation than a conventional VCO design. From Fig. 4b, the phase noise measurement results are $PN_H = -103$ dBc/Hz at 1 MHz and $PN_L = -109$ dBc/Hz at 1 MHz. PN_L is lower than PN_H by 6 dB, which matches with the frequency division theory.

Conclusion: For the first time, a prototype CMOS DMVCO with injection locking is successfully implemented to demonstrate the idea. We could employ the higher mode to drive a mixer and the lower mode to drive the PLL feedback divider.

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