

# Integrated circuit transmission-line transformer power combiner for millimetre-wave applications

A.M. Niknejad, M. Bohsali, E. Adabi and B. Heydari

A new approach for power combining several low-voltage CMOS amplifiers using a new on-chip transmission line transformer structure is presented. The power combiner utilises the interconnection of short sections of integrated differential lines and has an efficiency independent of the transformation ratio. Full-wave electromagnetic simulation confirms the operation and low insertion loss of the transformer.

**Introduction:** One of the key challenges to the realisation of a fully integrated CMOS transceiver is the realisation of the power amplifier in a low-voltage CMOS process. The requirements for high-speed operation, namely short channel length and thin gate oxide, are fundamentally at odds with high-power capability, determined in large part by the breakdown voltage of the technology. Two issues limit the output power of CMOS transistors, especially at millimetre (mm)-wave frequencies. For a low-voltage transistor to realise high output power impedance transformation is required in order to transform down the antenna impedance to a sufficiently low value. In essence, by utilisation of a very large FET, one can deliver power by using a large current instead of voltage. Typical LC resonant matching networks, however, suffer from a trade-off between matching ratio and insertion loss. So there is a practical limit to the output power determined by the losses incurred in the matching network.

Recently demonstrated transformer power combining networks [1–3] have the advantage that they can transform the load at constant insertion loss nearly independent of the matching ratio. This is a very important advantage for CMOS technology, which suffers from relatively lossy passive devices owing to the conductive substrate and thin metal layers. Compare the loss of a classic Wilkinson combiner to a transformer-based system. If a corporate ladder structure is employed, the loss increases logarithmically with the number of stages  $N$ :

$$P_{out} = \gamma^{\log_2 N} NP_o$$

where  $\gamma$  is the insertion loss of each stage, and  $P_o$  is the output power of each amplifier. For example, assuming  $P_{out}/P_o = 10$  when  $\gamma = 1$  dB requires 32 stages with an overall efficiency of only 33%. In comparison, a single-stage combining network has an efficiency of about 80%. On the other hand, an  $N$ -way Wilkinson power combiner suffers high losses so that  $\gamma_N > \gamma$ , resulting in no net improvement of efficiency. In a transformer-based combiner, all the power stages combine simultaneously and the loss is, to first order, only a function of the individual transformer loss, which is typically 1 dB for on-chip optimised structures.

**Transmission-line balun combiner:** In the proposed combiner, each pair of coupled lines forms a transmission-line transformer. At lower frequencies the lines can be realised using coupled inductors. At higher frequencies, however, differential transmission lines are used instead. As shown in Fig. 1, one end of the line is excited in single-ended fashion (although differential drive is possible and preferable), while at the tail end of the line the odd-mode voltages are summed in phase to form a voltage across a balanced or unbalanced load. The purpose of the balun is to convert a signal referenced to ground into a balanced ‘floating’ voltage. Since a single-ended drive excites both even- and odd-mode waves, it is important to create a line with large even-mode impedance  $Z_{oe}$  in order to suppress this unwanted mode. The odd-mode impedance, on the other hand, should equal the source impedance in order to obtain a match.

To realise a mm-wave amplifier, each transistor is first scaled up as much as feasible in order to obtain sufficient gain. Then  $N$  transistors each drive a pair of lines forming a balanced transmission line. The lines are connected at the load so that the load current flows through all structures, whereas the voltages at the tail end of the line sum appropriately. The load of  $NZ_{oo}$  is therefore transformed down to an impedance of  $Z_{oo}$ . This structure is easily implemented on-chip by placing the tails of the transmission lines in close proximity to allow easy interconnection of the lines. The inputs of the lines are separated to minimise parasitic coupling between the lines. The length of the lines should be kept as small as practical to minimise the line losses. Unlike a conventional balun

employing 90° sections, lines as short as 5–10° have been simulated and show good performance. This is important for two reasons: size and hence cost for an integrated balun, and performance (insertion loss).

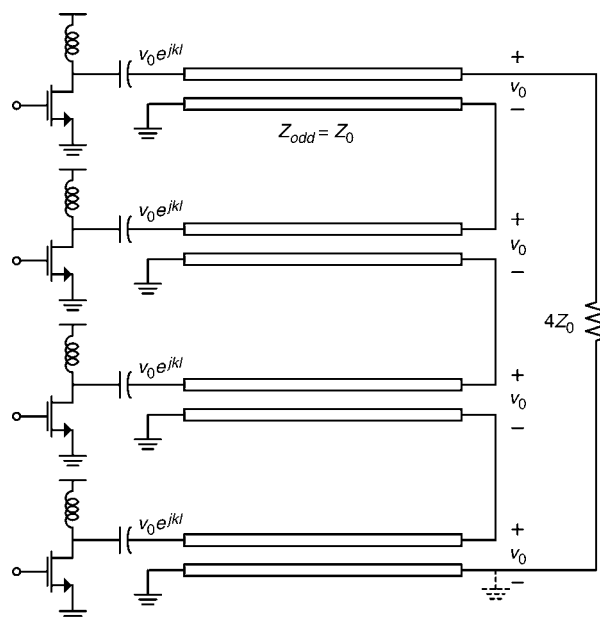


Fig. 1 Transmission-line transformer-based power combining allows low-voltage stages to sum power into a load efficiently

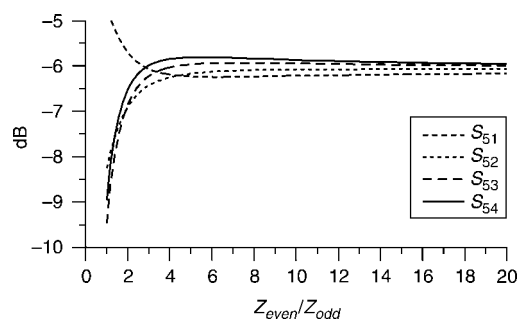


Fig. 2 Magnitude of coupled power (dB) from four-way power combiner against normalised even-mode impedance; lines excited in differential mode

**Simulation results:** To verify the functionality of this structure, a circuit level simulation was performed. Ideal lines are modelled with Agilent ADS coupled lines. Fig. 2 shows the magnitude of the coupling terms  $S_{Sx}$ , where four lines are joined to power combine. Here a relatively short 10° line is employed with varying even-mode impedance. For larger even-mode impedance, the line behaves as desired, approaching perfect power summation (–6 dB). To improve the performance of the combiner, a ‘floating’ differential drive is preferred. In a single-ended drive, impractically large values of  $Z_{oe}/Z_{oo}$  are required. In the design of the combiner, the gap spacing is chosen to appropriately fashion the odd-mode impedance

$$Z_{odd} = \sqrt{\frac{L - M}{C_0 + 2C_c}}$$

where  $L$  and  $M$  are the line self and mutual inductance per unit length, and  $C_0$  and  $C_c$  are the line-to-ground and line-to-line coupling capacitance per unit length. The even-mode impedance is given by

$$Z_{even} = \sqrt{\frac{L + M}{C_0}}$$

For good performance, we wish to maximise the ratio of  $Z_{even}$  to  $Z_{odd}$ :

$$\frac{Z_{even}}{Z_{odd}} = \sqrt{\frac{L + M C_0 + 2C_c}{L - M C_0}}$$

As  $k \rightarrow 1$  and  $C_0 \rightarrow 0$ , this ratio tends to infinity. In practical differential lines, the coupling factor  $k \sim 0.7$ , and common-mode impedance is a strong function of how the even-mode return current flows through the structure. At high frequencies the return current in the substrate is very lossy and must return to the source through substrate contacts (e.g. transistors body terminals and explicit substrate taps). To maximise the even-mode impedance, these substrate taps should be placed as far away from the structure as possible. Furthermore, the transistor ground connections should be isolated with chokes.

Full-wave electromagnetic simulation (ADS Momentum) is used to predict the high-frequency performance of the structure. The simulations are calibrated to measurement results by choosing appropriate dielectric loss and resistivity so as to match measurements of co-planar transmission lines up to 65 GHz. The combiner is implemented in a generic digital 90 nm CMOS process, utilising the top-most metal layer to maximise the distance to the substrate (thickness of 1 and 5.5  $\mu\text{m}$  oxide beneath metal). Coupled lines with  $W = 5 \mu\text{m}$  and gap spacing  $S = 0.5 \mu\text{m}$  are used in the design. In this simulation substrate contacts were placed 100  $\mu\text{m}$  away from each terminal of the lines to simulate the practical situation. It is important to use two separate contacts at each end to simulate the return current flow. The simulated values for the setup result in  $Z_{oo} = 28 \Omega$  and  $Z_{oe} = 123 \Omega$ .

Using the full-wave simulation results of the coupled lines of length 200  $\mu\text{m}$ , a four-way combiner has been simulated. The simulation setup is shown in Fig. 3, where each line is excited differentially. Chokes of 600 pF have been used to isolate the ground from the balanced lines. A load equal to  $4Z_s$  is driven by each stage, with  $Z_s = Z_{oo}$  initially, and then optimised to minimise the insertion loss. The final source impedance is  $Z_s = 34 \Omega$ . The achievable performance for the device is an insertion loss of 1.09 dB, shown in Fig. 4. The insertion loss varies by only 0.16 dB over the band of interest 55–65 GHz. While a high impedance mm-wave antenna can be easily fabricated, for practical situations a 50  $\Omega$  load is preferred. By employing broadside coupling one can lower the odd-mode impedance.

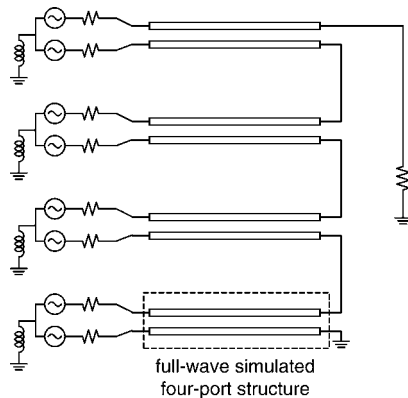


Fig. 3 Simulation setup for combined full-wave and circuit simulation of four-way combiner

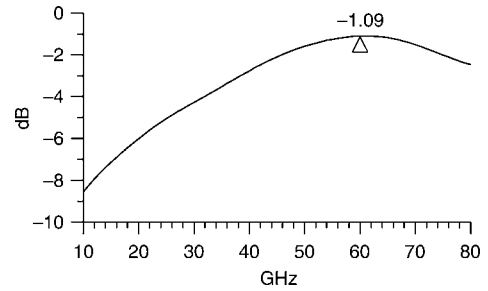


Fig. 4 Combined full-wave and circuit simulation of four-way combiner insertion loss

**Conclusions:** By utilising a new transmission-line transformer layout, a structure compatible with standard digital CMOS process, we have demonstrated an efficient and compact layout for a mm-wave power combiner. The power combiner allows full integration of matching and combining networks on the CMOS die, which allows a fully integrated CMOS mm-wave power amplifier to be realised.

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